NEC

MOS INTEGRATED CIRCUIT

μPD6125A, 6126A

4-BIT SINGLE CHIP MICROCONTROLLER FOR REMOTE CONTROL TRANSMISSION

DESCRIPTION

The μPD6125A and 6126A are 4-bit single-chip microcontrollers for infrared remote controllers for TVs, VCRs, stereos, cassette decks, air conditioners, etc.

These microcontrollers consist of ROM, RAM, a 4-bit parallel-processing ALU, a programmable timer, key input/output ports, and transmit output ports. Functioning is controlled in software.

FEATURES

- Transmitter for programmable infrared remote controller
- 19 types of instructions
- Instruction execution time: 17.6 μs (with 455-kHz ceramic oscillator)
- Program memory (ROM) capacity: 1002 × 10 bits
- Data memory (RAM) capacity: 32 × 5 bits
- 9-bit programmable timer: 1 channel
- I/O pins ($K_{I/O}$): 8 pins
- I/O pins (I/O)
  - μPD6125A: 4 pins
  - μPD6126A: 8 pins
- Input pins (K_I): 4 pins
- Serial input pins (S-IN): 1 pin
- Transmission-in-progress indication pin (S-OUT): 1 pin
- Transmit carrier frequency (REM)
  fosc/12, fosc/8
- Standby operation (HALT/STOP mode)
- Low power consumption
- Current consumption in STOP mode (T_A = 25°C)
  1 μA MAX.
- Low-voltage operation: V_{DD} = 2.0 to 6.0 V

Caution To use the NEC transmission format, ask NEC to supply the custom code.
The mask option (PLA data) setting of μPD6125A, μPD6126A is different from that of the μPD6125, 6126.

★ **When a register is used as the operand of a branch instruction, do not use R_0.**

The information in this document is subject to change without notice.

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Printed in Japan

The mark ★ shows major revised points.

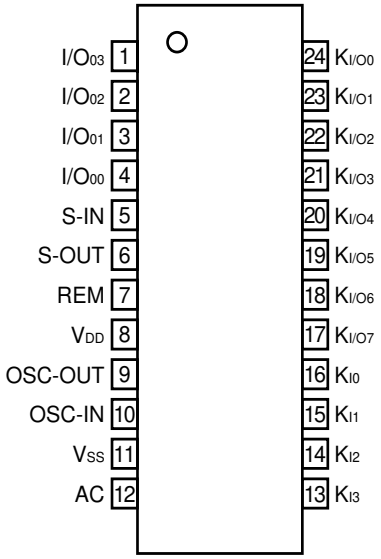
ORDERING INFORMATION

Part Number	Package
μPD6125ACA-XXX	24-pin plastic shrink DIP (300 mil)
μPD6125AG-XXX	24-pin plastic SOP (300 mil)
μPD6126AG-XXX	28-pin plastic SOP (375 mil)

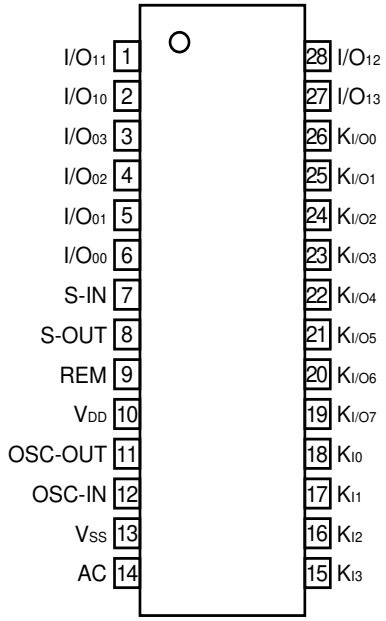
Remark XXX indicates a ROM code suffix.

PIN CONFIGURATION (Top View)

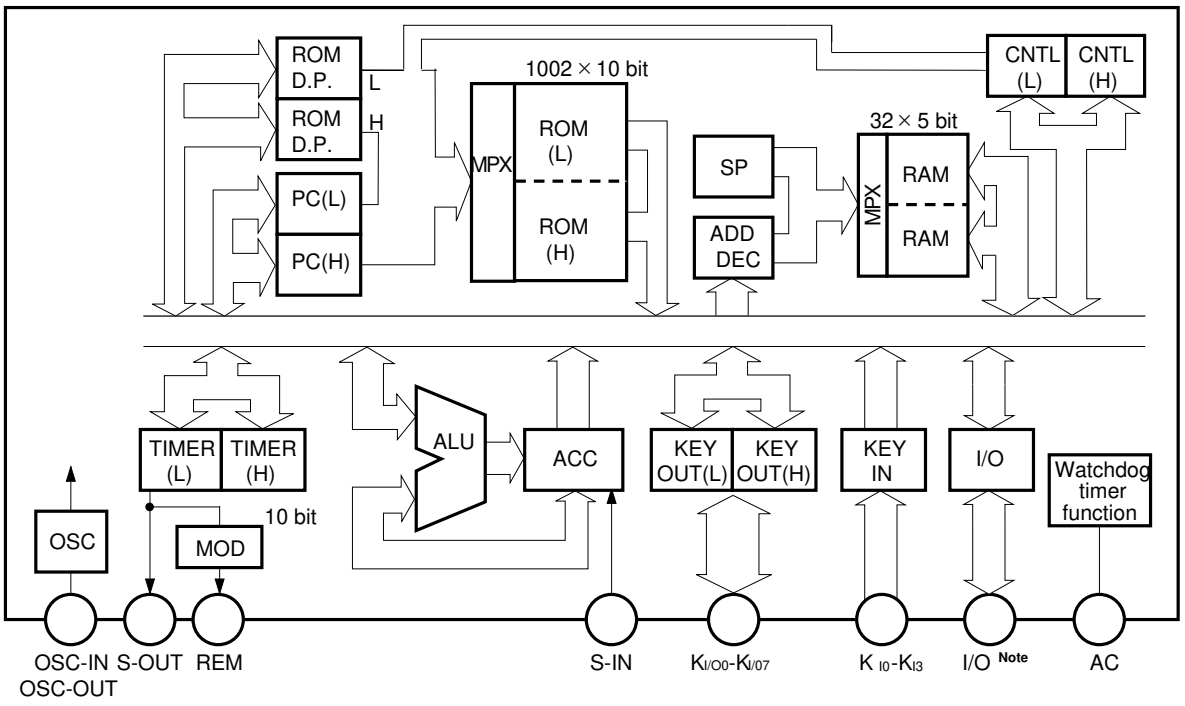
• μPD6125A



• μPD6126A



BLOCK DIAGRAM



Note μPD6125A: I/O_{00}-I/O_{03}
μPD6126A: I/O_{00}-I/O_{03}, I/O_{10}-I/O_{13}

DIFFERENCES AMONG PRODUCTS

Item \ Part Number	μPD6125A	μPD6126A
ROM capacity	1002 × 10 bits (Mask ROM)	
RAM capacity	32 × 5 bits	
I/O pins	12 ($K_{I/O0-7}$, I/O_{00-03})	16 ($K_{I/O0-7}$, I/O_{00-03}, I/O_{10-13})
S-IN pins	Provided	
Current consumption (f_{OSC} = STOP) (MAX.)	1 μA	
S-IN high level input current (MAX.)	15 μA	
Transmit carrier frequency	$f_{OSC}/12$, $f_{OSC}/8$	
Low-voltage detection (reset) circuit	Not provided	
Supply voltage	V_{DD} = 2.0 to 6.0 V	
Package	• 24-pin plastic SOP (300 mil) • 24-pin plastic shrink DIP (300 mil)	• 28-pin plastic SOP (375 mil)

1. PROGRAM COUNTER (PC) ..... 10 BITS

The program counter (PC) is a binary counter, which holds the address information for the program memory.

Figure 1-1. Program Counter Organization

PC_9	PC_8	PC_7	PC_6	PC_5	PC_4	PC_3	PC_2	PC_1	PC_0	PC

Normally, the program counter contents are automatically incremented each time an instruction is executed, according to the number of instruction bytes.

When executing a jump instruction (JMP0, JC, JF), the program counter indicates the jump destination.

Immediate data or the data memory contents are loaded to all or some bits of the PC.

When executing the call instruction (CALL0), the PC contents are incremented (+1) and saved into the stack memory. Then, a value needed for each jump instruction will be loaded.

When executing the return instruction (RET), the stack memory contents are double incremented (+2) and loaded into the PC.

When “all clear” is input or on reset, the PC contents are cleared to “000H”.

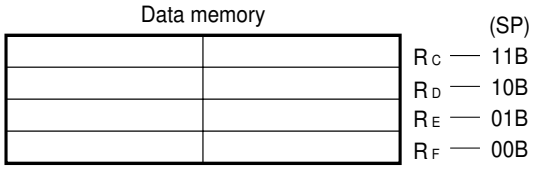
2. STACK POINTER (SP) ..... 2 BITS

This 2-bit register holds the start address information for the stack area. The stack area is shared with the data memory.

The SP contents are incremented, when the call instruction (CALL0) is executed. They are decremented, when the return instruction (RET) is executed.

The stack pointer is cleared to “00B” after reset or “all clear” is input, and indicates the highest address FH for the data memory as the stack area.

The figure below shows the relationship for the stack pointer and the data memory area.

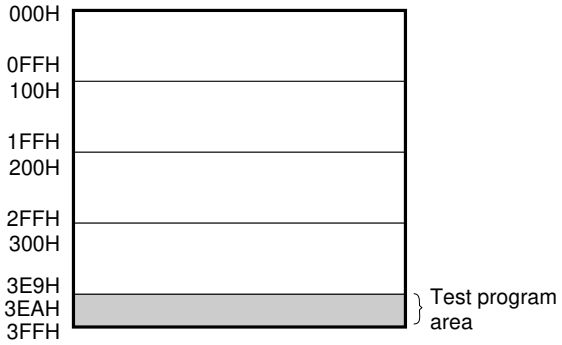


If the stack pointer overflows or underflows, it is determined that the CPU overflows, and the PC internal reset signal will be generated.

3. PROGRAM MEMORY (ROM) ..... 1002 STEPS × 10 BITS

The program memory (ROM) is configured in 10 bits steps. It is addressed by the program counter. Program and table data are stored in the program memory.

Figure 3-1. Program Memory Map

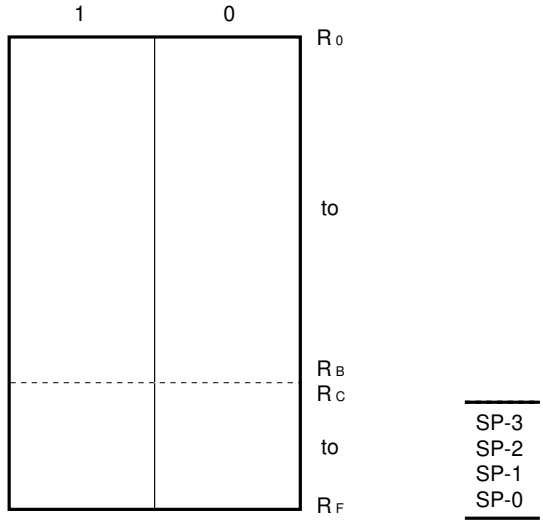


4. DATA MEMORY (RAM) ..... 32 WORDS × 5 BITS

The data memory is a RAM of 32 words × 5 bits. The data memory stores processing data. In some cases, the data memory is processed in 8-bit units. R_0 may be used as the data pointer for the ROM.

After power application, the RAM will be undefined. The RAM retains the previous data on reset.

Figure 4-1. Data Memory Organization



Caution Avoid using the RAM areas R_D, R_E, and R_F in a CALL routine as much as possible because these areas are also used as stack memory areas (to prevent program hang-up in case the value of the SP is destroyed due to some reason such as noise).

When using these RAM areas as general-purpose RAM areas, be sure to include stack pointer checking in the main routine.

5. DATA POINTER (R_0)

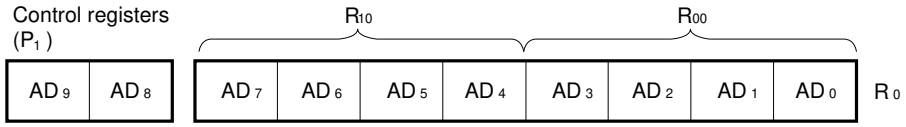
R_0 (R_{10}, R_{00}) for the data memory can serve as the data pointer for the ROM.

R_0 specifies the low-order 8 bits in the ROM address. The high-order 2 bits in the ROM address are specified by the control register.

Table referencing for ROM data can be easily executed by calling the ROM contents by setting the ROM address to the data pointer.

When “all clear” is input or on reset, it becomes undefined.

Figure 5-1. Data Pointer Organization

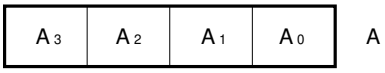


6. ACCUMULATOR (A) ..... 4 BITS

The accumulator (A) is a 4-bit register. The accumulator plays a major role in each operation.

When “all clear” is input or on reset, it becomes undefined.

Figure 6-1. Accumulator Organization



7. ARITHMETIC LOGIC UNIT (ALU) ..... 4 BITS

The arithmetic logic unit (ALU) is a 4-bit operation circuit, and executes simple operations, such as arithmetic operations.

8. FLAGS

(1) Status flag

When the status for each pin is checked by the STTS instruction, if the condition coincides with the condition specified by the STTS instruction, the status flag (F) is set (to 1).

When “all clear” is input or on reset, it becomes undefined.

(2) Carry flag

When the INC (increment) instruction or the RL (rotate left) instruction is executed, if a carry is generated from the MSB for the accumulator, the carry flag (C) is set (to 1).

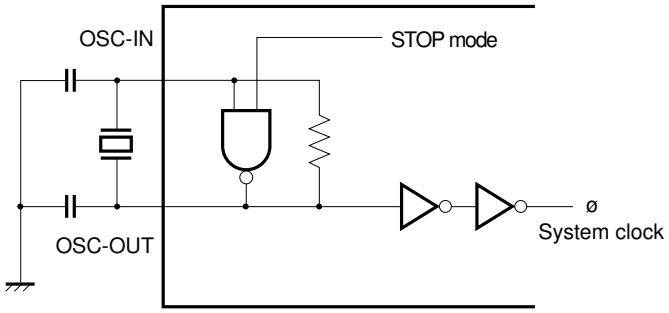
The carry flag (C) is also set (to 1), if the contents for the accumulator are “FH”, when the SCAF instruction is executed.

When “all clear” is input or on reset, it becomes undefined.

9. SYSTEM CLOCK GENERATION CIRCUIT

The system clock generation circuit consists of an oscillation circuit, which uses a ceramic resonator (400kHz to 500kHz).

Figure 9-1. System Clock Generation Circuit



In the STOP mode (oscillation stop HALT instruction), the oscillation circuit in the system clock generation circuit stops its operation, and the system clock ø is stopped.

10. TIMER

The timer block determines the transmission output pattern. The timer consists of 10 bits, of which 9 bits serve as the 9-bit down counter and the remaining 1 bit serves as the 1-bit latch, which determines the carrier output validity.

The 9-bit down counter is decremented (-1) every 8/fosc(s) in synchronization with the machine cycle, after starting down count operation. Down counting stops after all of the 9 bits become 0. When down counting is stopped, the signal indicating that the timer operation has stopped, is output. If the CPU is at standby (HALT TIMER) for the timer operation completion, the standby (HALT) condition is released and the next instruction will be executed. If the next instruction again sets the value of the down counter, down counting continues without any error (the carrier output of the REM pin is not affected).

Set the down count time according to the following calculation; (set value (HEX) + 1) x 8/fosc. Setting the value to the timer is done by the timer manipulation instruction.

When the down counter is operating, the remote control transmission carrier can be output to the REM pin. Whether or not to output the carrier can be selected by the MSB for the timer register block. Set "1", when outputting the carrier, or "0", when not outputting the carrier.

If all the down counter bits become "0", when outputting the carrier, the carrier output will be stopped. When not outputting the carrier, the REM pin output will become low level.

A signal in synchronization with the REM output is output to the S-OUT pin. However, the waveform for the S-OUT pin is low, when the carrier is being output to the REM pin, or it is high, when the carrier is not being output to the REM pin.

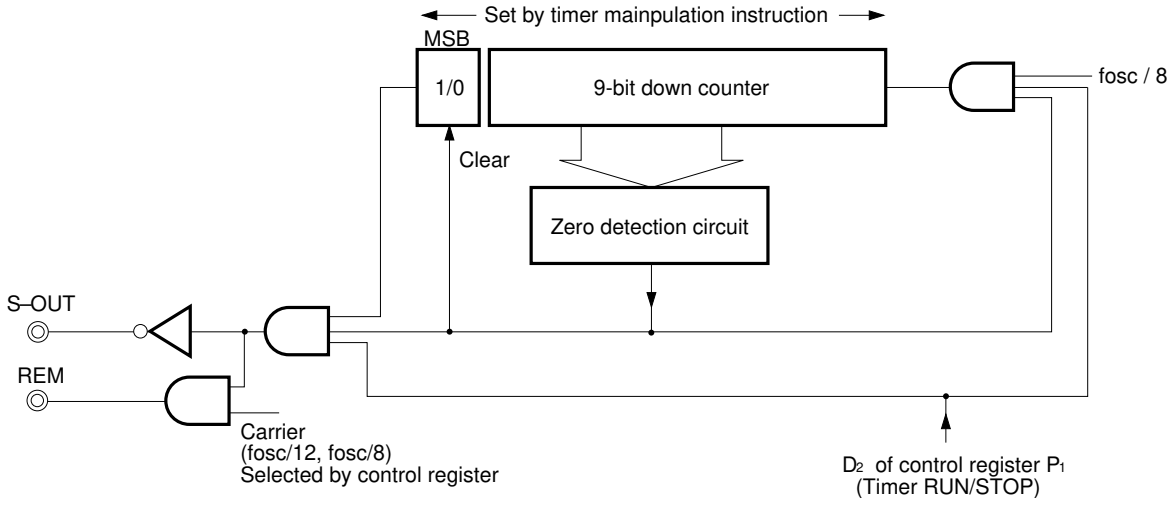
If the HALT instruction, which initiates the oscillation stop mode, is executed when the down counter is operating, the oscillation stop mode is initiated after down counting is stopped (after 0).

Timer operation STOP/RUN is controlled by the control register (P_1). (Refer to 13. CONTROL REGISTER (P_1).)

When "all clear" is input or on reset, the REM pin goes low and S-OUT pin goes high. All 10 bits of the timer are cleared to 000H.

Caution Because the timer clock is not synchronized with the carrier output, the pulse width may be shortened at the beginning and end of the carrier output.

Figure 10-1. Timer Block Organization



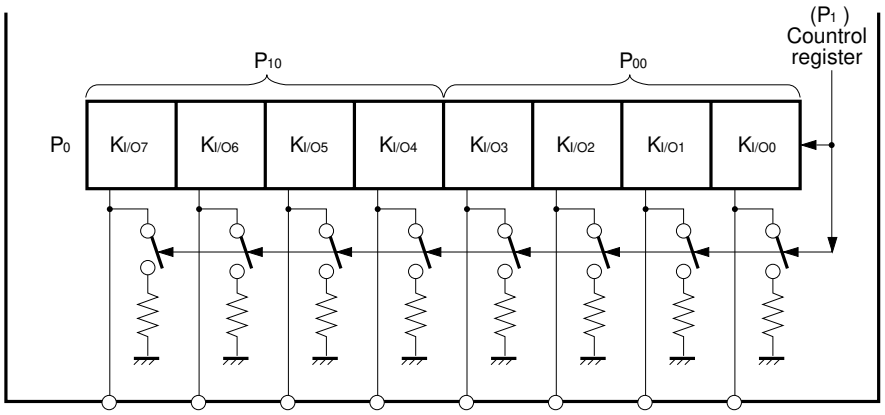
11. PIN FUNCTIONS

11.1 $K_{I/O}$ Pin (P_0)

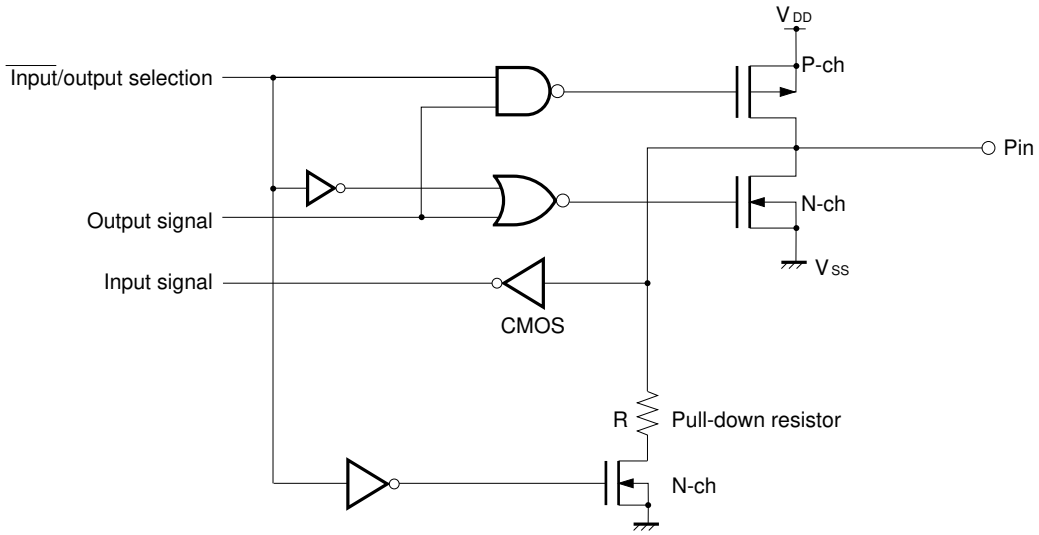
This is the 8-bit I/O pin for key-scan output. When the control register (P_1) is set for the input port, the port can be used as an 8-bit input pin. When the port is set for the input mode, all of these pins are pulled down to the V_{SS} level inside the LSI.

When "all clear" is input or on reset, input/output mode goes into effect, and the value of output latch becomes undefined.

Figure 11-1. $K_{I/O}$ Pin Organization



11.2 $K_{I/O}$ Pull-Down Resistor Organization



When $K_{I/O}$ is set to the input mode, pull-down resistor R is turned on.

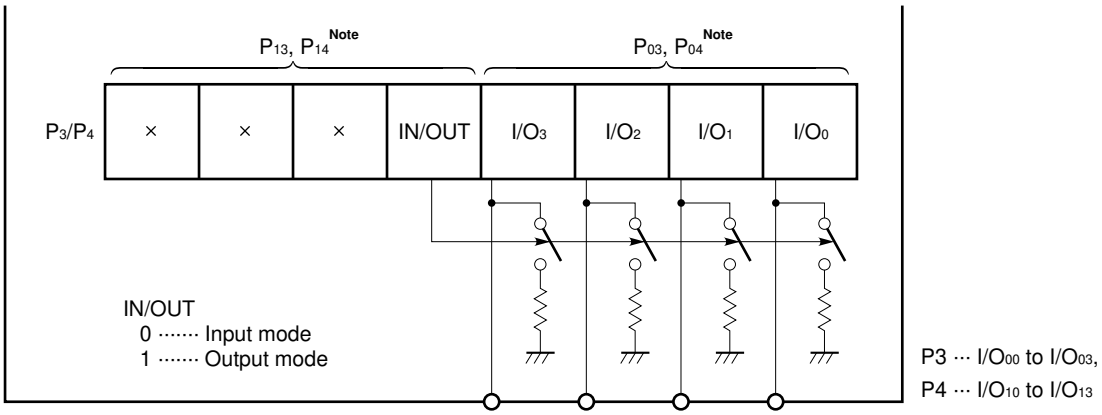
11.3 I/O Pin (P_3, P_4 Note)

P_3/P_4 are input/output pins for adding a key matrix. The LSB of control registers P_{13} and P_{14} switches between input and output modes.

When in input mode, all pins are pulled down by the LSI to the V_{SS} level.

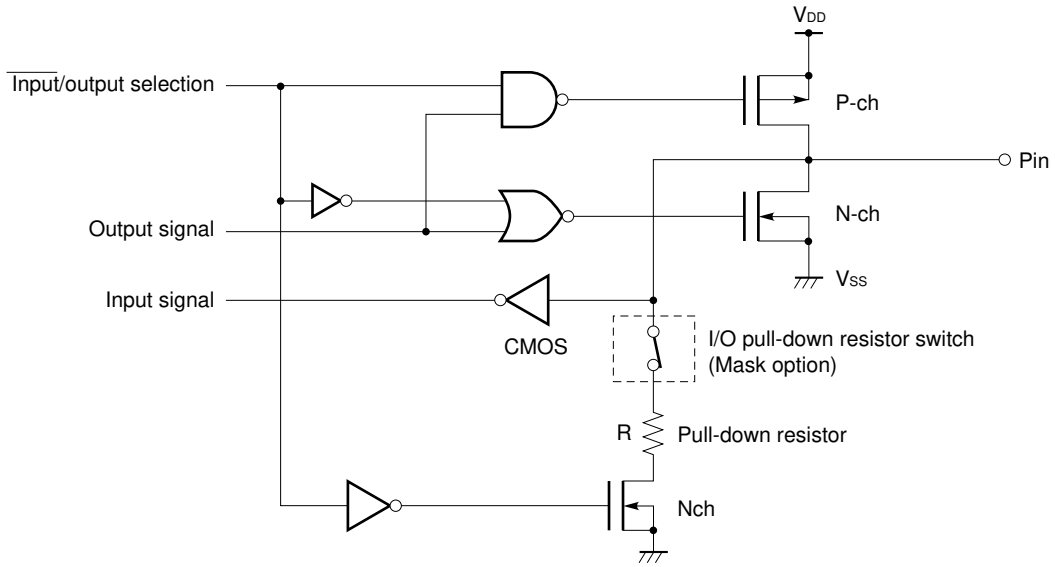
When "all clear" is input or on reset, input mode goes into effect, and the output latch value becomes undefined.

Figure 11-2. I/O Pin Organization



Note μPD6125A is not equipped with P_{13}, P_{14}, P_{03}, and P_{04}.

11.4 I/O Pull-Down Resistor Organization



The use of pull-down resistors for I/O can be selected by using the mask option.

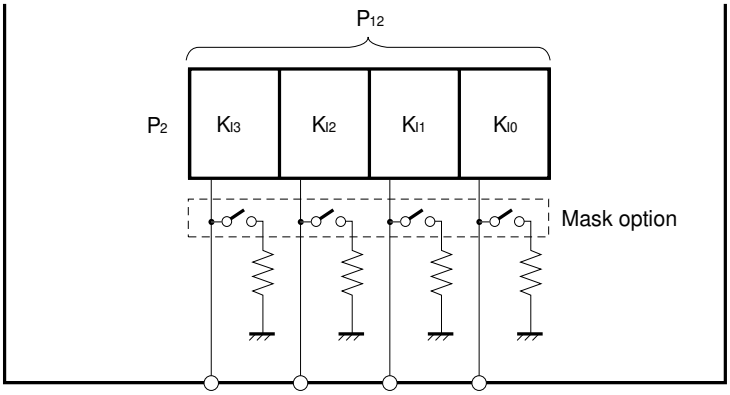
When the pull-down resistor switch is turned on (1 is set) by the mask option, the pull-down resistor R is turned on only in input mode.

Caution When using the pins as key switches, turn on the pull-down resistor switch by the mask option.

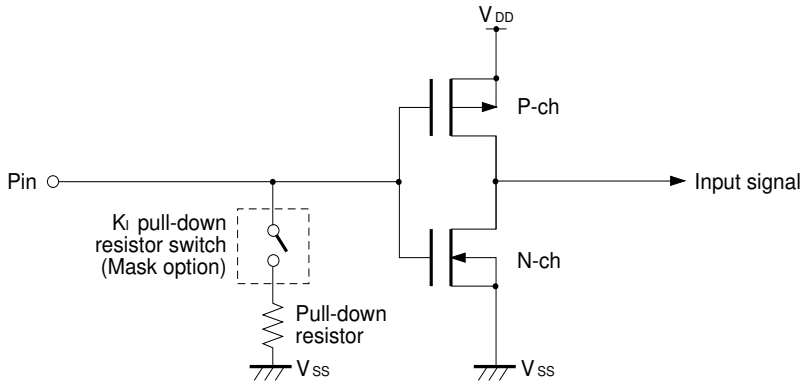
11.5 K_I Pin (P_{12})

This is the 4-bit pin for key input. All of these pins can be pulled down to the V_{SS} level by mask option.

Figure 11-3. K_I Pin Organization



11.6 K_I Pull-Down Resistor Organization



When the pull-down resistor switch is turned on (set 1) by the mask option, pull-down resistor R is turned on.

Caution When using the pin as the key switch, turn on the pull-down resistor switch by the mask option.

11.7 S-OUT Pin

By going low whenever the carrier frequency is output from the REM pin, the S-OUT pin indicates that communication is in progress.

★ The S-OUT pin is a CMOS output pin.

The S-OUT pin goes high on reset.

11.8 S-IN Pin (D_0 Bit of P_1)

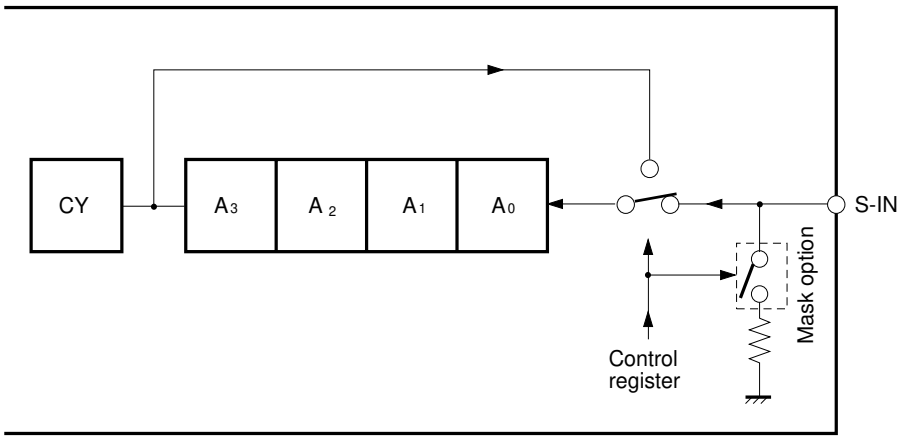
To input serial data, use the S-IN pin. When control register (P_1) is set to serial input mode, the S-IN pin is connected as an input to the LSB of the accumulator. The S-IN pin can be pulled down to the V_{SS} level by a mask option from within the LSI. In this state, if the rotate-left accumulator instruction (RL A) is executed, the data on the S-IN pin is copied to the LSB of the accumulator.

If the control register is released from serial input mode, the S-IN pin goes into a high-impedance state, but no through current flows internally.

When the RL A instruction is executed, the MSB is copied to the LSB.

When “all clear” is input or on reset, the S-IN pin goes into a high-impedance state.

Figure 11-4. The S-IN Pin Organization



12. PORT REGISTER (P×)

$K_{I/O}$, I/O, K_I, and the control register are handled as port registers.
The table below shows the relations between the port registers and pins.

Table 12-1. Relations between Port Registers and Pins

Pin Name	Input Mode		Output Mode		On Reset
	Read	Write	Read	Write	
$K_{I/O}$	Pin status	Output latch	Pin status	Output latch	Undefined [I/O mode, output latch]
K_I	Pin status	–	–	–	Input mode
I/O_0	Pin status	Output latch	Pin status	Output latch	Input mode
I/O_1					Output latch is undefined.
S-IN	Pin status is read by RL A instruction when D_0 of P_1 register = 1.				High impedance (D_0 of P_1 register = 0)

$P_1 \times$ (H)		$P_0 \times$ (L)	
$K_{I/O7-4}$ P_{10}		$K_{I/O3-0}$ P_{00}	P_0
Control register (H) P_{11}		Control register (L) P_{01}	P_1
K_{I3-0} P_{12}		— P_{02}	P_2
— P_{13}	IN/OUT	I/O_0 P_{03}	P_3
— P_{14}	IN/OUT	I/O_1 P_{04}	P_4

Caution The μPD6125A is not equipped with I/O_{10}-I/O_{13} pins.

13. CONTROL REGISTER (P_1)

The control register contains of 10 bits. The controllable items are shown in Table 13-1.

Table 13-1. Control Register (P1)

Bit		D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
Name		Test mode		–	HALT	D.P. AD_9	D.P. AD_8	MOD	Timer	$K_{I/O}$	RL A_{CC} $A_0 \leftarrow$
Set Value	0	Be sure to reset to 0.			NOP	AD_9=0	AD_8=0	f_{OSC}/8	STOP	IN	A_3
	1				OSC STOP	AD_9=1	AD_8=1	f_{OSC}/12	RUN	OUT	S-IN

D_0 ..... Specifies data to be input to A_0 when the accumulator is shifted to the left.
0: A_3, 1: S-IN

D_1 ..... Specifies the status of $K_{I/O}$, as follows:
0: input mode, 1: output mode

D_2 ..... Specifies the status of the timer, as follows:
0: Count stop, 1: Count execution

D_3 ..... Specifies the carrier frequency output from the REM pin.
0: f_{OSC}/8, 1: f_{OSC}/12

D_4, D_5 ..... Specify the high-order 2 bits of the ROM data pointer.

D_6 ..... Determines what happen to the oscillation circuit when the HALT instruction is executed.
0: Oscillation does not stop
1: Oscillation stops (STOP mode)

D_7 ..... Be sure to reset this bit to 0.

D_8, D_9 ..... These bits specify test modes. Be sure to reset them to 0.

Remark $D_0 = D_8 = D_9 = 0$ on reset, and the other bits are undefined.

14. STANDBY FUNCTION (HALT INSTRUCTION)

The μPD6600A is provided with the standby mode (HALT instruction), in order to reduce the power consumption, when not executing the program. Clock oscillation can be stopped in the standby mode (STOP mode).

In the standby mode, the program execution stops. However, the contents of the internal registers and the data memory are all retained.

14.1 STOP Mode (Oscillation Stop HALT Instruction)

In the STOP mode, the operation of the system clock generation circuit (ceramic resonator oscillation circuit) stops. Therefore, operations requiring the system clock will stop.

If the HALT instruction is executed during timer operation, the program counter stops. The oscillation stop mode will be initiated, after the timer count down operation is completed.

14.2 HALT Mode (Oscillation Continue HALT Instruction)

The CPU stops its operation, until the HALT release condition is satisfied.

The system clock operation continues in this mode.

14.3 Standby Release Conditions

(1) S-IN input
(2) $K_{I/O}$ input
(3) K_I input
(4) Timer count down operation completion
(5) I/O input
(6) K_I, I/O input

Remark Either high level or low level can be specified for setting a release condition by input.

Table 14-1. Standby Mode Releasing Condition

D_3	D_2	D_1	D_0	Releasing Condition	Remarks
0/1	0	0	0	S-IN	When RL ← A_3 is selected, the standby mode is always released.
	0	0	1	$K_{I/O}$	Valid only in the IN mode.
	0	1	0	K_I	
0	0	1	1	Timer	Released when 0.
0/1	1	0	0	I/O_0	Valid only in the IN mode.
	1	0	1	I/O_1	
1	1	1	0	K_I, I/O_0, I/O_1	Judged as an error and initialized even if one of the I/O is in OUT mode.

↳ Releasing condition: "0"···Low level detection
"1"···High level detection

Caution μPD6125A is not equipped with I/O_{10} - I/O_{13} pins.

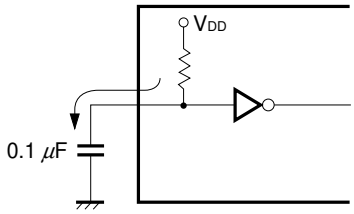
15. AC PIN (ALL CLEAR PIN)

Internal part of the CPU including the program counter can be reset by setting the AC pin to the low level.

Watchdog Timer Function

A power-on reset function and a CR watchdog timer function, that can be controlled by program, can be realized by connecting a 0.1 μF capacitor across the AC pin and the V_{SS}.

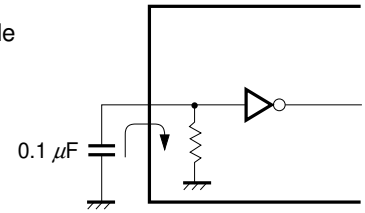
Charge mode



Charge start instruction

Execute HALT instruction immediately before NOP. (Charge for 0.4 ms or more)

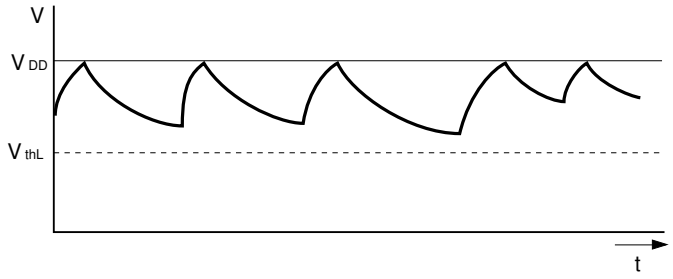
Discharge mode



Discharge start instruction

Discharge starts after the NOP instruction execution. (Discharge time is about 5 ms from V_{DD} to V_{th})

Charge-discharge pattern



The pattern must be controlled by the program, in such a manner that the C charge level will not go below V_{thL} .

Caution When the watchdog timer function is not used, switch to charging mode by executing a NOP instruction immediately before a HALT instruction at the beginning of the program. (Be sure to connect the capacitor.)

16. MASK OPTIONS (PLA DATA)

The following items can be selected by mask option selection:

- Provide/not provide K_I, I/O, S-IN pin pull-down resistor
- Carrier duty selection (1/2, 1/3) at fosc/12
- Hang-up detection specification

Mask option data should be registered at the object code end.

BIT Assignment by Switch Selection

Address	Corresponding Portion	MSB							LSB
		7	6	5	4	3	2	1	0
0	K_I pull-down resistor	K_{I0}	K_{I1}	K_{I2}	K_{I3}	0			
1	Duty S-IN	0	0	0	Duty selection	0	0	S-IN pull-down resistor	0
2	Hang up detection	$K_{I/O}$ ALL	HALT S-IN	HALT $K_{I/O}$	HALT K_I	HALT I/O_0	HALT I/O_1	I/O_0 ALL	I/O_1 ALL
3	I/O_0 pull-down resistor	I/O_{00}	I/O_{01}	I/O_{02}	I/O_{03}	0			
4	I/O_1 pull-down resistor	I/O_{10}	I/O_{11}	I/O_{12}	I/O_{13}	0			

Caution μPD6125A is not equipped with I/O_{10} - I/O_{13} pins.

Switch for Data

(1) Pull-down resistor
When 0 ··· Not provided (OFF)
When 1 ··· Provided (ON)

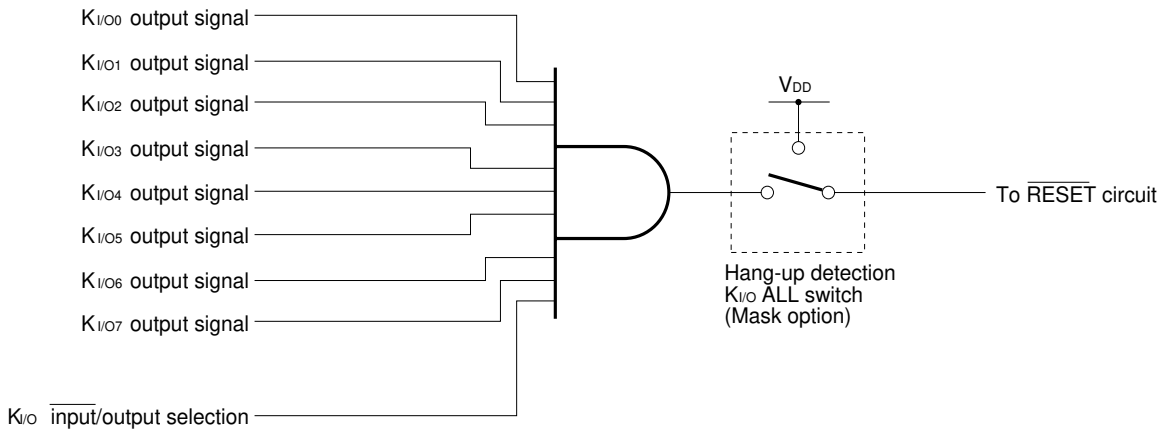
(2) Modulation duty (at fosc/12)
When 0 ··· 1/2 duty
When 1 ··· 1/3 duty

(3) Hang-up detection

<1> $K_{I/O}$ ALL, I/O_0 ALL, I/O_1 ALL
If the switch for hang-up detection $K_{I/O}$ ALL (I/O_0 ALL, I/O_1 ALL) is set to ON (1) by mask option, the system is reset, if in oscillation HALT (STOP) mode, the $K_{I/O}$ (I/O_0, I/O_1) pin is in input mode, or if at least one of the $K_{I/O}$ (I/O_0, I/O_1) pins is low (AC pin discharge mode).
When 0 ··· No reset function (OFF)
When 1 ··· Reset function (ON)

Caution To use a pin as a key source of a key matrix, be sure to set the switch to ON by mask option.

Figure 16-1. Hang-up Detection $K_{I/O}$ ALL Organization



Remark The above is also applicable to I/O_0 ALL, I/O_1 ALL.

<2> HALT releasing condition specification (S-IN, $K_{I/O}$, K_I, I/O_0, I/O_1)

If the condition specified by mask option to be unused is satisfied in the HALT mode, the system is reset.

When 0 ··· Used

When 1 ··· Unused

Caution Be sure to specify the HALT mode of the unused releasing condition to be unused (set).

17. PROGRAM DEVELOPMENT TOOLS

To develop programs for the μPD6125A, 6126A, an assembler and an emulator for the μPD612X series are available from I.C. Corp. For details, contact IC Corp.

18. ORDERING ROM CODE

<1> To generate the data required for ordering a mask ROM, after assembling the program, convert the HEX file to a ROM file by using the PROM utility program "UPDPROM".

Caution When using "UPDPROM" select "27256" for PROM TYPE.

<2> Confirm that the instruction ROM code data is stored in addresses 0 through 7D3H of the PROM. Also confirm that the mask option ROM code data are stored in the following addresses.

μPD6125A: Addresses 7FF0H through 7FF3H
μPD6126A: Addresses 7FF0H through 7FF4H

19. INSTRUCTION SET

Accumulator Manipulation Instructions

	R_r	–	R_{10}	R_{11}	R_{12}		R_{1F}	R_{00}	R_{01}		R_{0F}
ANL	A, R_r		D00	D01	D02		D0F	D20	D21		D2F
ANL	A, @R_0H	D10									
ANL	A, @R_0L	D30									
ANL	A, #data	D31									
ORL	A, R_r		E00	E01	E02		E0F	E20	E21		E2F
ORL	A, @R_0H	E10									
ORL	A, @R_0L	E30									
ORL	A, #data	E31									
XRL	A, R_r		A00	A01	A02		A0F	A20	A21		A2F
XRL	A, @R_0H	A10									
XRL	A, @R_0L	A30									
XRL	A, #data	A31									
INC	A	A13									
RL	A	F13									

Input/Output Instructions

	P_P	P_{10}	P_{11}	P_{12}	P_{13}	P_{14}	P_{00}	P_{01}	P_{02}	P_{03}	P_{04}
IN	A, P_P	F18	F19	F1A	F1B	F1C	F38	F39	F3A	F3B	F3C
OUT	P_P, A	218	219	21A	21B	21C	238	239	23A	23B	23C
ANL	A, P_P	D18	D19	D1A	D1B	D1C	D38	D39	D3A	D3B	D3C
ORL	A, P_P	E18	E19	E1A	E1B	E1C	E38	E39	E3A	E3B	E3C
XRL	A, P_P	A18	A19	A1Z	A1B	A1C	A38	A39	A3A	A3B	A3C

	P_P	P_0	P_1	P_2	P_3	P_4
OUT	P_P #data	318	319	31A	31B	31C

P_{1P} and P_{0P} operate in pair format

Data Transfer Instructions

	R_r		R_{10}	R_{11}	R_{12}		R_{1F}	R_{00}	R_{01}		R_{0F}
MOV	A, R_r		F00	F01	F02		F0F	F20	F21		F2F
MOV	A, @R_0H	F10									
MOV	A, @R_0H	F30									
MOV	A, #data	F31									
MOV	R_r, A		200	201	202		20F	220	221		22F

	R_r		R_0	R_1	R_2		R_F
MOV	R_r, #data		300	301	302		30F
MOV	R_r, @R_0		320	321	322		32F

R_{1r} and R_{0r} operate in pair format

Branch Instructions

	R_r	–	R_0	R_1	R_2		R_F
	JMP0 addr	411					
★	JMP0 R_r Note	–	–	401	402		40F
	JC addr	611					
	JC R_r Note	–	–	601	602		60F
	JNC addr	631					
	JNC R_r Note	–	–	621	622		62F
	JF addr	711					
	JF R_r Note	–	–	701	702		70F
	JNF addr	731					
	JNF R_r Note	–	–	721	722		72F

← Pair register

★ **Note** r = 1 – F
r = 0 cannot be used.

Subroutine Instructions

CALL0 addr	312	411
RET	412	

Timer/Counter Manipulation Instructions

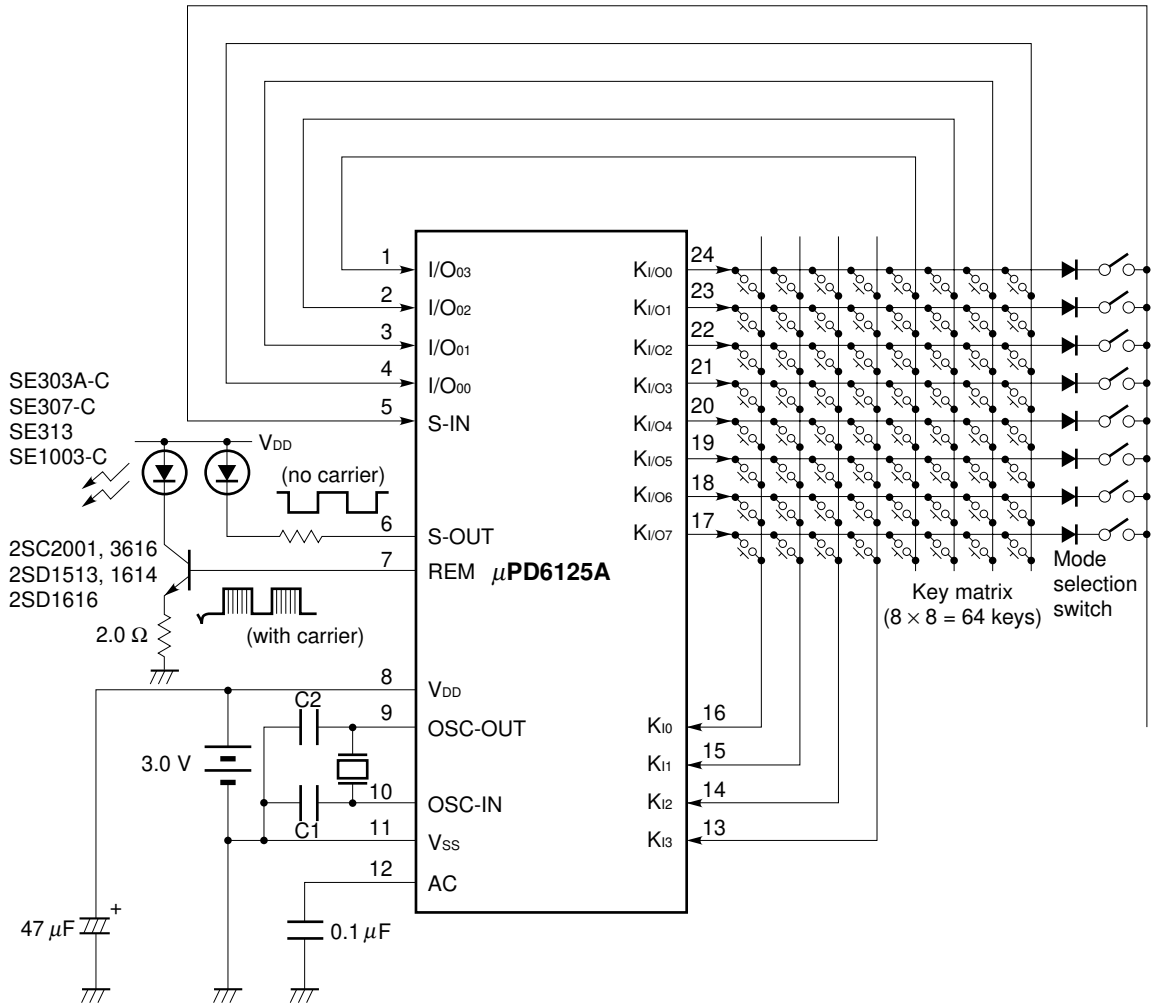
	T_t	$T_{0\text{-}1}$	T_1	T_0
MOV A, T_t		–	F1F	F3F
MOV T_t, A			21F	23F
MOV T, #data		31F		
MOV T, @R_0		33F		

Other Instructions

		R_{00}	R_{01}	R_{02}		R_{0F}
HALT #data	111					
STTS R_{0r}		120	121	122		12F
STTS #data	131					
SCAF	D13					
NOP	000					

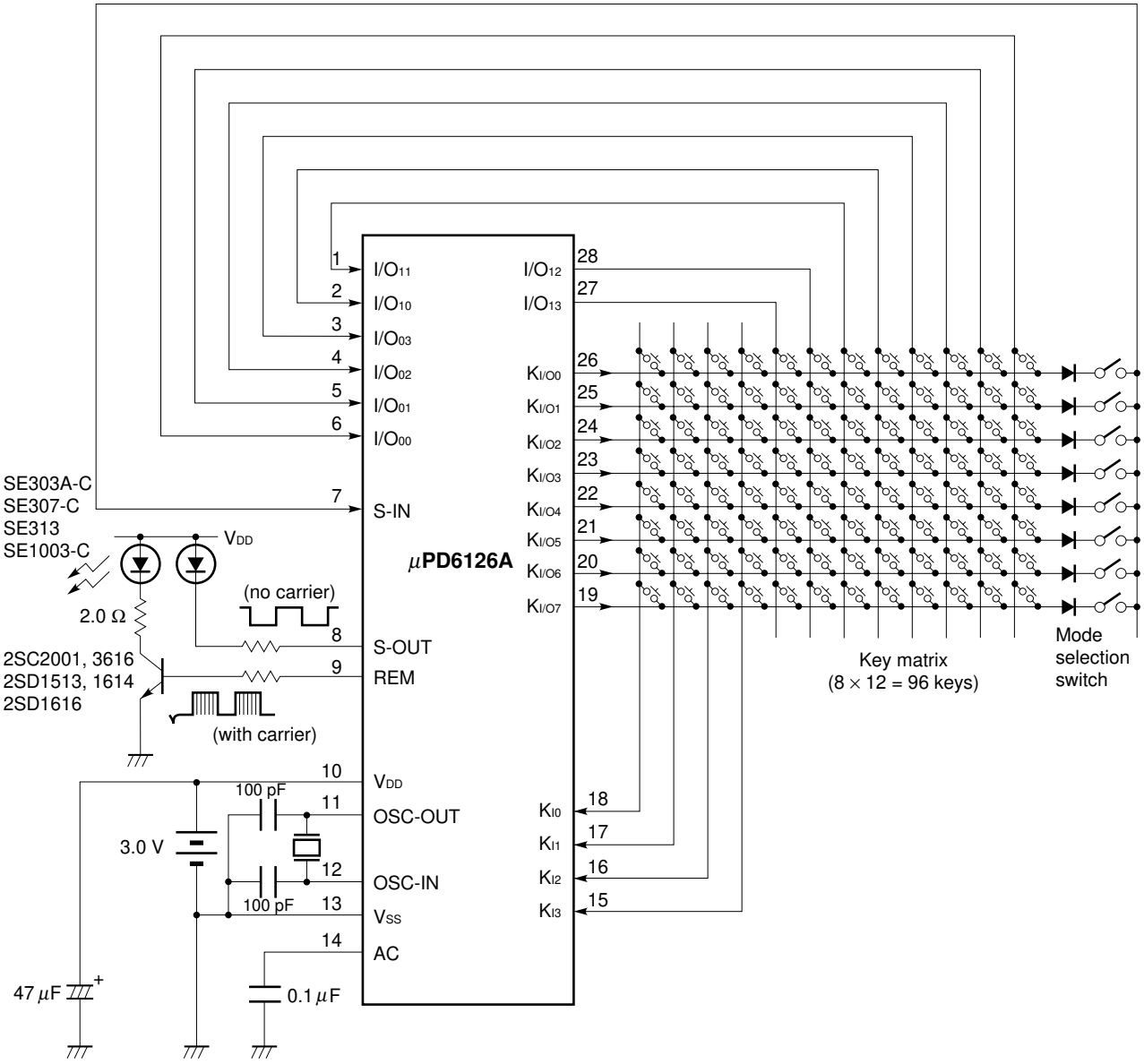
20. TYPICAL APPLICATION CIRCUIT EXAMPLE

(1) μPD6125A application circuit example



Caution The ceramic resonator start-up capacitor value must be determined, by taking the voltage level and the oscillation start-up characteristics for the ceramic resonator into consideration.

(2) μPD6126A application circuit example



Caution The ceramic resonator start-up capacitor value must be determined, by taking the voltage level and the oscillation start-up characteristics for the ceramic resonator into consideration.

21. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings (T_A = 25 °C)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	–0.3 to +7.0	V
Input voltage	V_{IN}	–0.3 to V_{DD}+0.3	V
Operating ambient temperature	T_A	–20 to +75	°C
Storage temperature	T_{stg}	–40 to +125	°C

★ **Caution If the rated value of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. Absolute maximum ratings therefore specify the values exceeding which the product may be physically damaged. Never exceed these values when using the product.**

Recommended Operating Range (T_A = –20 to +75 °C)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}	2.0		6.0	V
Oscillation frequency	f_{OSC}	400		500	kHz

DC Characteristics (V_{DD} = 3.0V, f_{OSC} = 455kHz, T_A = 25 °C)

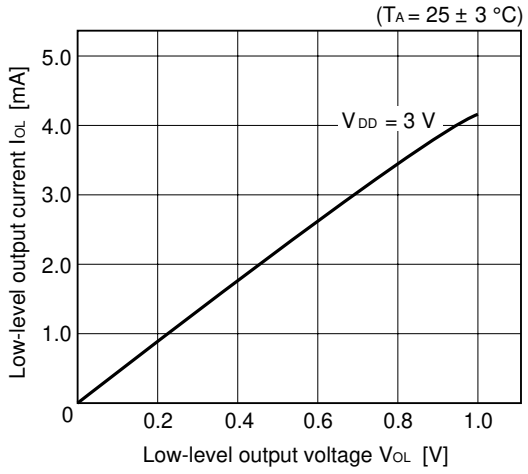
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{DD}		2.0		6.0	V
Current dissipation 1	I_{DD1}	f_{OSC} = 455 kHz		0.3	1.0	mA
Current dissipation 2	I_{DD2}	f_{OSC}= STOP			1.0	μA
REM high level output current	I_{OH1}	V_O = 1.0 V	–5	–8		mA
REM low level output current	I_{OL1}	V_O = 0.3 V	0.5	1.5	2.5	mA
S-OUT high level output current	I_{OH2}	V_O = 2.7 V	–0.3	–1.0	–2.0	mA
S-OUT low level output current	I_{OL2}	V_O = 0.3 V	1	1.5		mA
K_I high level input current	I_{IH1}	V_I = 3.0 V	10		30	μA
K_I high level input current	$I_{IH1'}$	V_I = 3.0 V, without pull-down resistor			0.2	μA
K_I low level input current	I_{IL1}	V_I = 0 V			–0.2	μA
$K_{I/O}$, I/O high level input current	I_{IH2}	V_I = 3.0 V	10		30	μA
$K_{I/O}$, I/O high level input current	$I_{IH2'}$	V_I = 3.0 V, without pull-down resistor			0.2	μA
$K_{I/O}$, I/O low level input current	I_{IL2}	V_I = 0 V			–0.2	μA
$K_{I/O}$, I/O high level output current	I_{OH3}	V_O = 2.5 V	–1.5	–2.0	–4.0	mA
$K_{I/O}$, I/O low level output current	I_{OL3}	V_O = 2.1 V	25	50	100	μA
K_I, I/O high level input voltage	V_{IH1}		2.1		3.0	V
K_I, I/O low level input voltage	V_{IL1}		0		0.9	V
$K_{I/O}$ high level input voltage	V_{IH2}		1.3		3.0	V
$K_{I/O}$ low level input voltage	V_{IL2}		0		0.4	V
AC pull-up resistor	R_1	V_I = 0 V	0.3		3.0	kΩ
AC pull-down resistor	R_2	V_I = 2.7 V	150	400	1500	kΩ
AC high level input voltage	V_{IH3}		1.8		3.0	V
AC low level input voltage	V_{IL3}		0		1.2	V

Recommended Ceramic Resonator

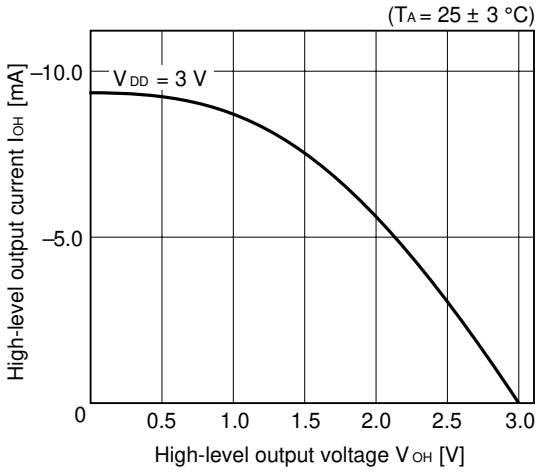
Manufacturer	Product	External Capacitance (pF)		Oscillation Voltage Range (V)		Remarks
		C1	C2	MIN.	MAX.	
Murata Mfg. Co., Ltd.	CSB375P	220	220	2.0	3.3	
	CSB400P	220	220	2.0	5.0	
	CSB455E	100	100	2.0	5.0	
	CSB480E	100	100	2.0	5.0	
	CSB500E	100	100	2.0	3.3	
Toko Ceramic Co., Ltd.	CRK400	100	100	2.0	6.0	
	CRK455	100	100	2.0	6.0	
	CRK500	100	100	2.0	6.0	

22. CHARACTERISTICS CURVE (Target Value)

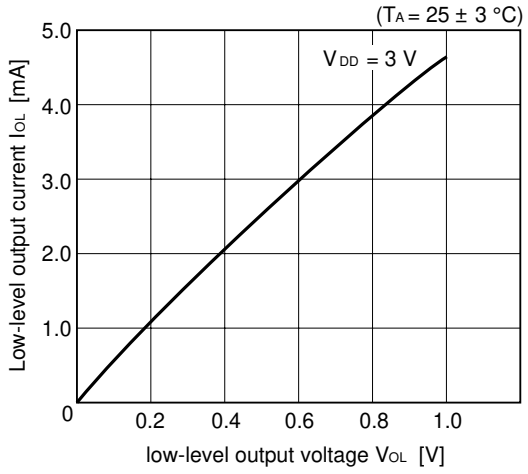
I_{OL} vs V_{OL} characteristic examples (REM)



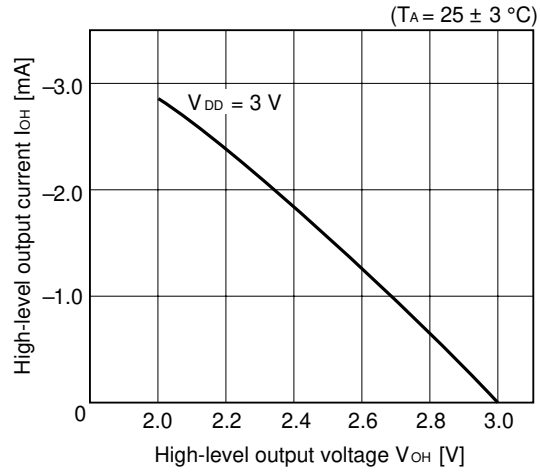
I_{OH} vs V_{OH} characteristic examples (REM)



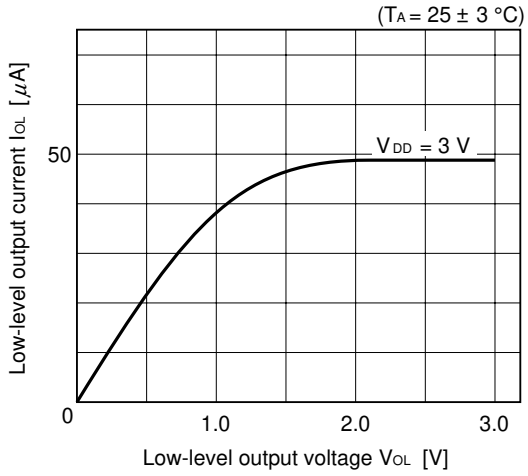
I_{OL} vs V_{OL} characteristic examples (S-OUT)



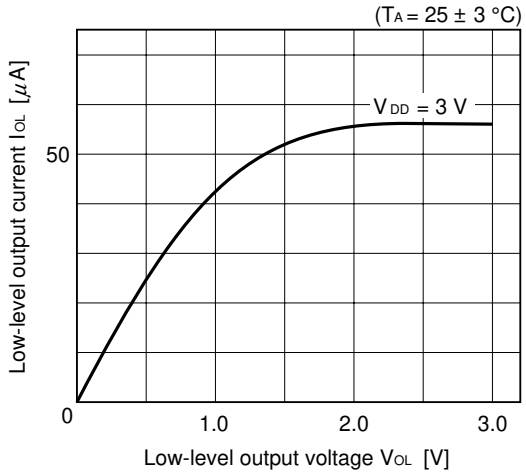
I_{OH} vs V_{OH} characteristic examples (S-OUT)



I_{OL} vs V_{OL} characteristic examples ($K_{I/O0}$-$K_{I/O3}$, I/O)

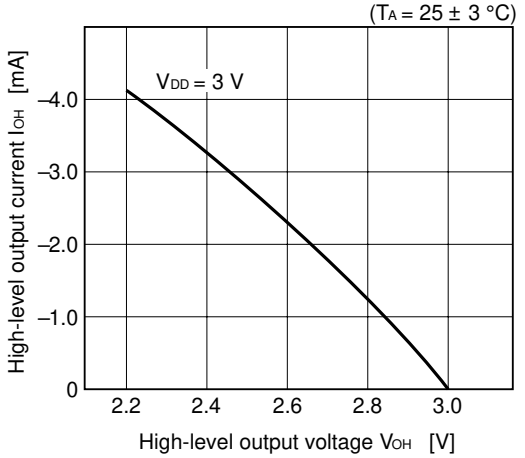


I_{OL} vs V_{OL} characteristic examples ($K_{I/O0}$-$K_{I/O7}$)



I_{OH} vs V_{OH} characteristic examples ($K_{I/O}$, I/O)

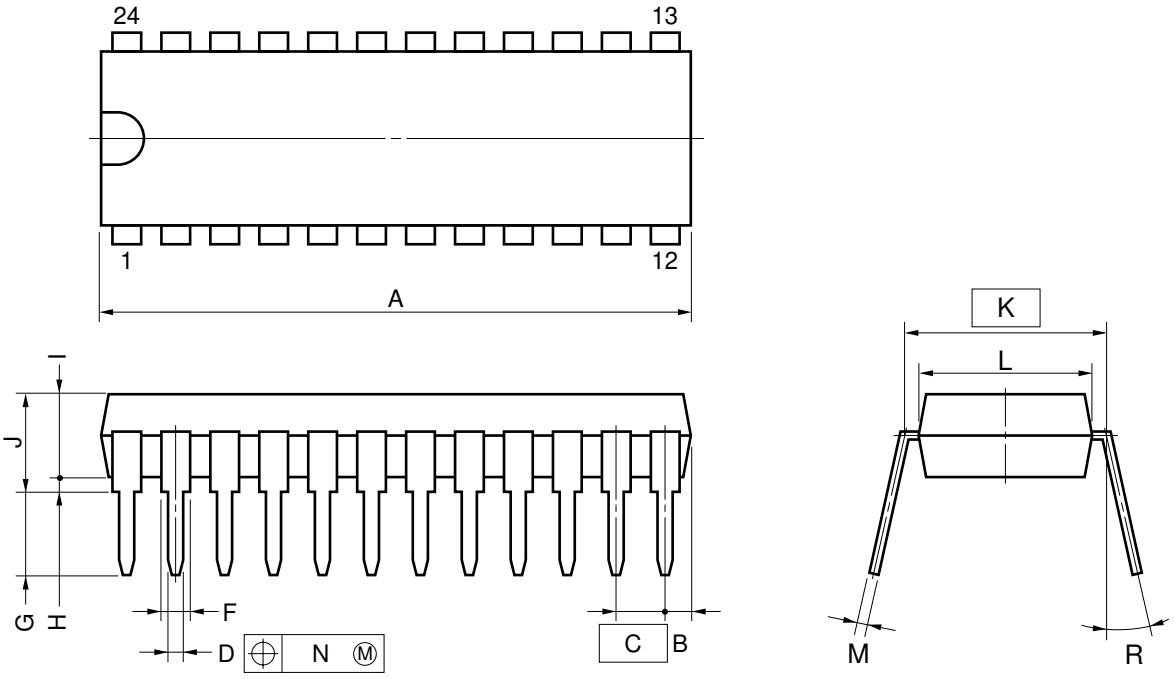
(T_A = 25 ± 3 °C)



23. PACKAGE DRAWINGS

(1) μPD6125A package drawings (1/2)

24 PIN PLASTIC SHRINK DIP (300 mil)



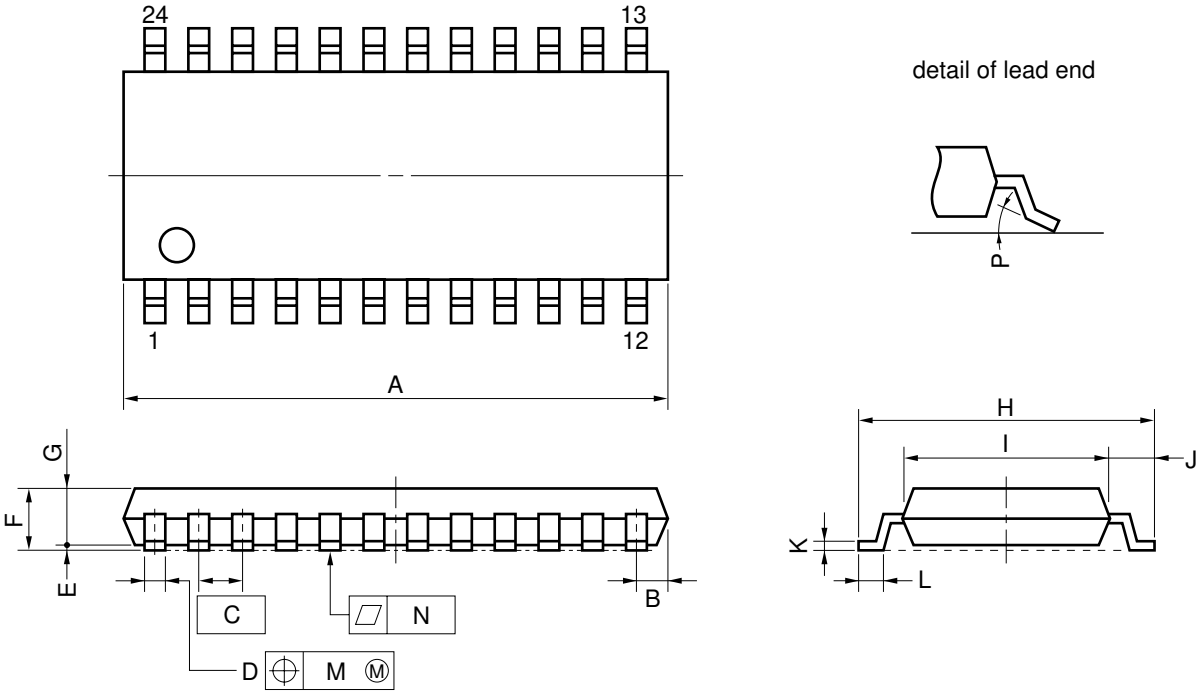
NOTE

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	23.12 MAX.	0.911 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	0.85 MIN.	0.033 MIN.
G	3.2 ± 0.3	0.126 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	7.62 (T.P.)	0.300 (T.P.)
L	6.5	0.256
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

S24C-70-300B-1

24 PIN PLASTIC SOP (300 mil)



NOTE

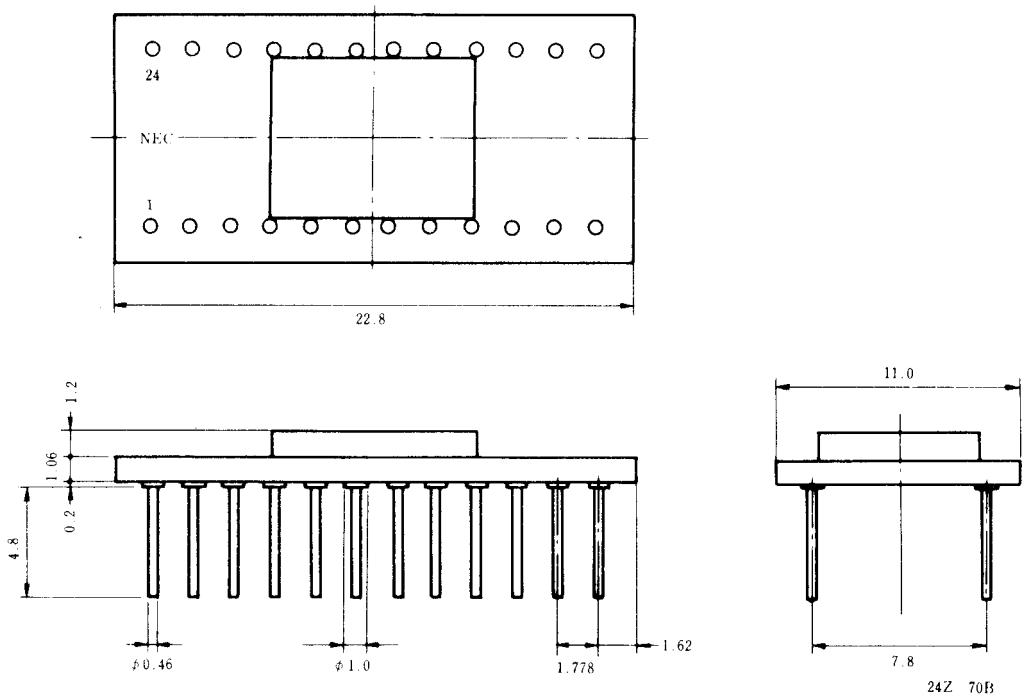
Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	15.54 MAX.	0.612 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1±0.1	0.004±0.004
F	1.8 MAX.	0.071 MAX.
G	1.55	0.061
H	7.7±0.3	0.303±0.012
I	5.6	0.220
J	1.1	0.043
K	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$
L	0.6±0.2	$0.024^{+0.008}_{-0.009}$
M	0.12	0.005
N	0.10	0.004
P	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$

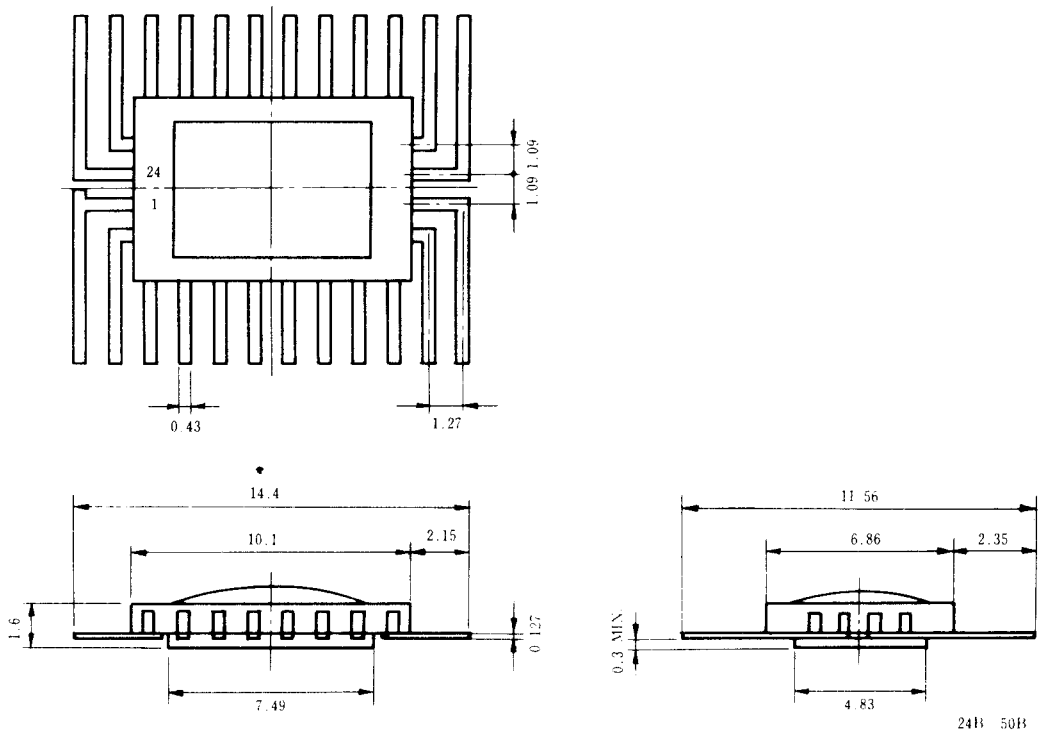
P24GM-50-300B-4

(1) μPD6125A package drawings (2/2)

24-PIN SHRINK DIP FOR ES (REFERENCE) (Unit in mm)

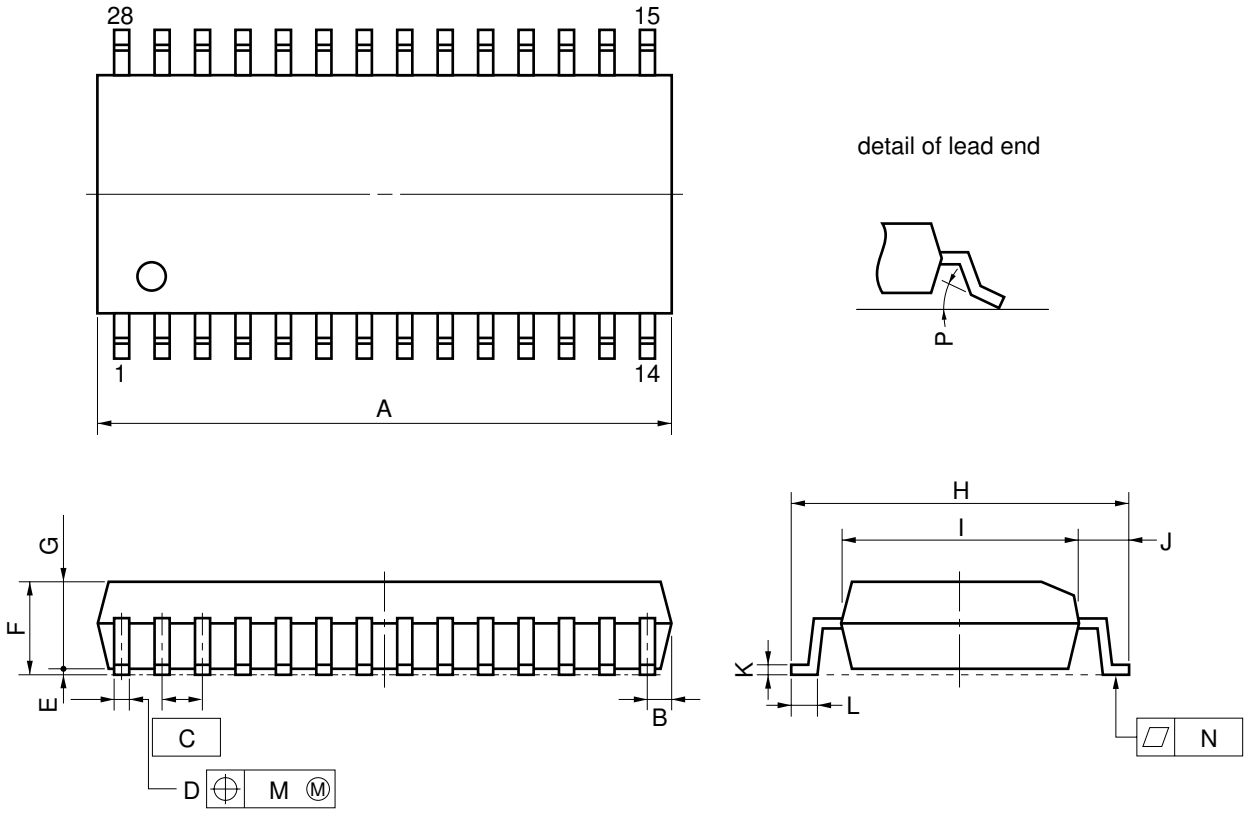


24-PIN CERAMIC MINI FLAT PACKAGE FOR ES (REFERENCE) (Unit in mm)



(2) μPD6126A package drawings (1/2)

28 PIN PLASTIC SOP (375 mil)



NOTE

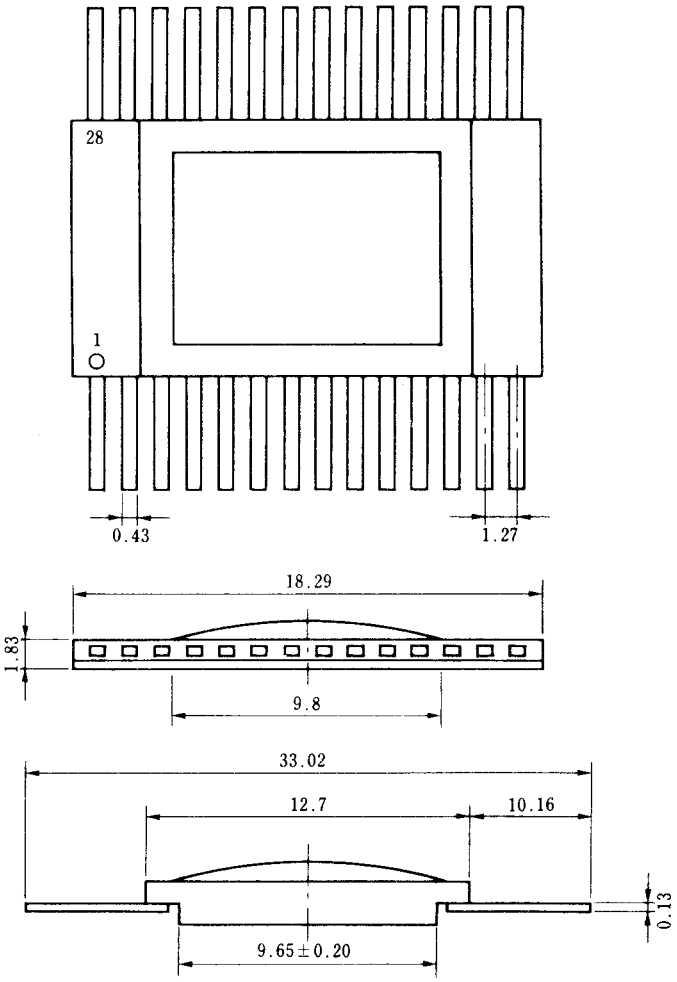
Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	18.07 MAX.	0.712 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1±0.1	0.004±0.004
F	2.9 MAX.	0.115 MAX.
G	2.50	0.098
H	10.3±0.3	$0.406^{+0.012}_{-0.013}$
I	7.2	0.283
J	1.6	0.063
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	0.12	0.005
N	0.15	0.006
P	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$

P28GM-50-375B-3

(2) μPD6126A package drawings (2/2)

28-PIN CERAMIC SOP FOR ES (REFERENCE) (Unit in mm)



24. RECOMMENDED SOLDERING CONDITIONS

It is recommended that μPD6125A and 6126A be soldered under the following conditions.

★ For details on the recommended soldering conditions, refer to Information Document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For other soldering methods and conditions, consult NEC.

Table 24-1. Surface-Mount Type Soldering Conditions

(1) μPD6125AG-XXX: 24-pin plastic SOP (300 mil)

Soldering Method	Soldering Conditions	Symbol for Recommended Condition
Infrared reflow	Package peak temperature: 230 °C, time: 30 seconds max. (210 °C min.), number of times: 1	IR30-00-1
VPS	Package peak temperature: 215 °C, time: 40 seconds max. (200 °C min.), number of times: 1	VP15-00-1
Partial heating	Pin temperature: 300 °C max., time: 3 seconds max. (per device side)	–

(2) μPD6126AG-XXX: 28-pin plastic SOP (375 mil)

Soldering Method	Soldering Conditions	Symbol for Recommended Condition
Infrared reflow	Package peak temperature: 230 °C, time: 30 seconds max. (210 °C min.), number of times: 1	IR30-00-1
VPS	Package peak temperature: 215 °C, time: 40 seconds max. (200 °C min.), number of times: 1	VP15-00-1
Wave soldering	Solder bath temperature: 260 °C max., time: 10 seconds max., number of times: 1 Pre-heating temperature: 120 °C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300 °C max., time: 3 seconds max. (per device side)	–

Caution Use more than one soldering method should be avoided (except in the case of partial heating).

Table 24-2. Insertion Type Soldering Conditions

μPD6125ACA-XXX: 24-pin plastic shrink DIP (300 mil)

Soldering Method	Soldering Conditions
Wave soldering (Only for pin)	Solder bath temperature: 260 °C max., time: 10 seconds max.
Partial heating	Pin temperature: 300 °C max., time: 3 seconds max. (per pin)

Caution Wave soldering is only for pins in order that jet solder can not contact with the chip directly.

APPENDIX μPD612X SERIES PRODUCTS

★

Item \ Part Number	μPD6124A	μPD6600A	μPD61P24	μPD6125A	μPD6126A
ROM capacity	1002 × 10 bits (Mask ROM)	512 × 10 bits (Mask ROM)	1002 × 10 bits (One-time PROM)	1002 × 10 bits (Mask ROM)	
RAM capacity	32 × 5 bits				
I/O pins	8 pins ($K_{I/O0-7}$)			12 pins ($K_{I/O0-7}$, I/O_{00-03})	16 pins ($K_{I/O0-7}$, I/O_{00-03}, I/O_{10-13})
S-IN pins	Provided				
Current consumption (f_{OSC} = STOP) (MAX.)	2 μA		1 μA		
S-IN high level input current (MAX.)	30 μA		15 μA		
Transmit carrier frequency	$f_{OSC}/12$, $f_{OSC}/8$				
Low-voltage detector (reset) circuit	Provided		Not provided		
Mask option	Provided		Not provided (Fixed)	Provided	
Supply voltage	V_{DD} = 2.0 to 5.5 V	V_{DD} = 2.2 to 3.6 V	V_{DD} = 2.2 to 5.5 V	V_{DD} = 2.0 to 6.0 V	
Package	• 20-pin plastic SOP (300 mil) • 20-pin plastic shrink DIP (300 mil)			• 24-pin plastic SOP (300 mil) • 24-pin plastic shrink DIP (300 mil)	• 28-pin plastic SOP (375 mil)

[MEMO]

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

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The application circuits and their parameters are for reference only and are not intended for use in actual design-ins.

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