

Silicon NPN Power Transistors

2SD1432

DESCRIPTION

- With TO-3P(H)IS package
- High voltage ,high speed
- Low collector saturation voltage

APPLICATIONS

- Designed for use in TV and CRT display horizontal output applications

PINNING

PIN	DESCRIPTION
1	Base
2	Collector
3	Emitter

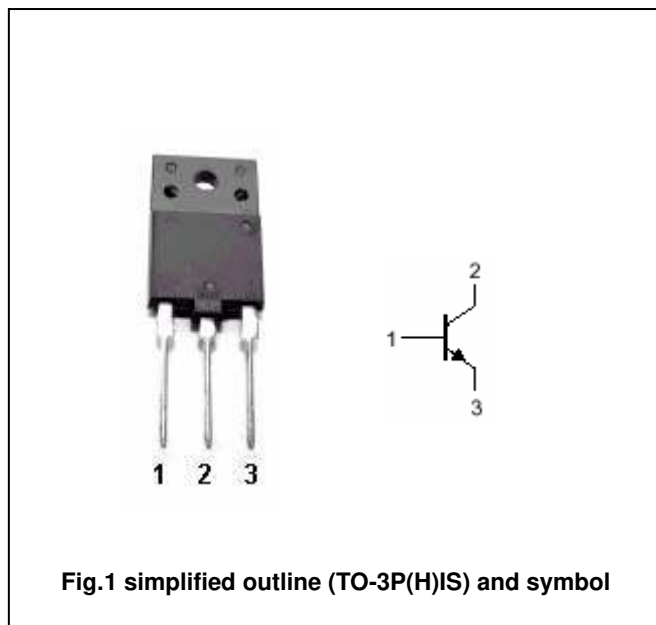


Fig.1 simplified outline (TO-3P(H)IS) and symbol

Absolute maximum ratings ($T_a=25^\circ\text{C}$)

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V_{CBO}	Collector-base voltage	Open emitter	1500	V
V_{CEO}	Collector-emitter voltage	Open base	600	V
V_{EBO}	Emitter-base voltage	Open collector	5	V
I_C	Collector current		6	A
P_D	Total power dissipation	$T_C=25^\circ\text{C}$	80	W
T_j	Junction temperature		150	$^\circ\text{C}$
T_{stg}	Storage temperature		-55~150	$^\circ\text{C}$

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CHARACTERISTICS

T_j=25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V _{CE(sat)}	Collector-emitter saturation voltage	I _C =5A; I _B =1A			5.0	V
V _{BE(sat)}	Base-emitter saturation voltage	I _C =5A; I _B =1A			1.5	V
I _{CBO}	Collector cut-off current	V _{CB} =500V; I _E =0			10	μ A
I _{EBO}	Emitter cut-off current	V _{EB} =5V; I _C =0			1	mA
h _{FE}	DC current gain	I _C =1A ; V _{CE} =5V	8			
f _T	Transition frequency	I _C =0.1A ; V _{CE} =10V		3		MHz
C _{OB}	Output capacitance	I _E =0 ; V _{CB} =10V;f=1.0MHz		165		pF
t _f	Fall time	I _C =5A;I _{B1} =1A			1.0	μ s

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PACKAGE OUTLINE

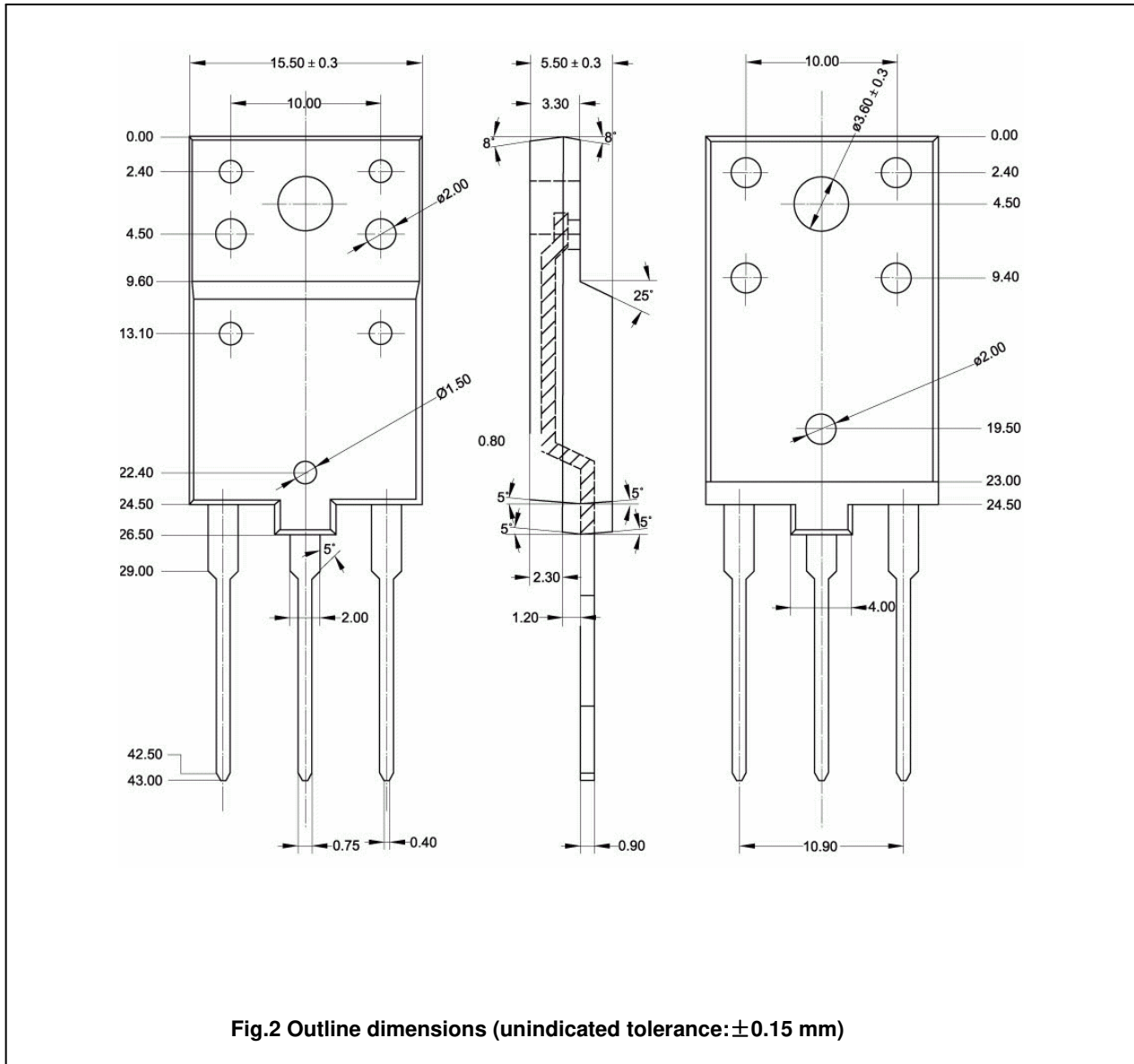


Fig.2 Outline dimensions (unindicated tolerance: ± 0.15 mm)