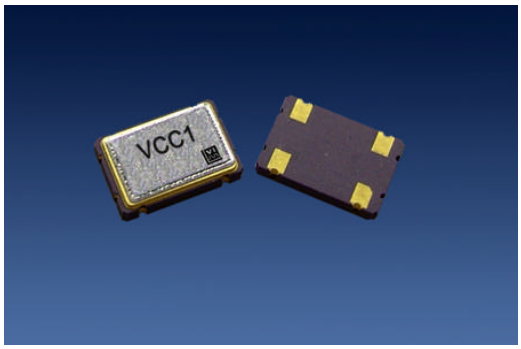
VCC1 series

1.8, 2.5, 3.3, 5.0 volt CMOS Oscillator



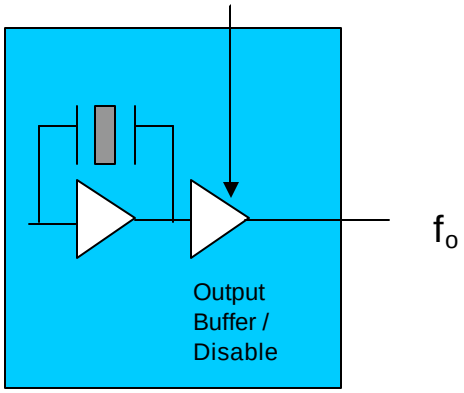
The VCC1 Crystal Oscillator

Features

- CMOS output
- Output frequencies to 190 MHz
- Low jitter, Fundamental or 3rd OT Crystal
- Tristate output for board test and debug
- -10/70 or –40/85 °C operating temperature
- Gold over nickel contact pads
- Hermetically sealed ceramic SMD package
- Product is compliant to RoHS directive and fully compatible with lead free assembly

Applications

- SONET/SDH/DWDM
- Ethernet, Gigabit Ethernet
- Storage Area Network
- Digital Video
- Broadband Access
- Microprocessors/DSP/FPGA



Description

Vectron's VCC1 Crystal Oscillator (XO) is quartz stabilized square wave generator with a CMOS output, operating off either a 1.8, 2.5, 3.3 or a 5.0 volt supply.

The VCC1 is uses fundamental or 3rd overtone crystals resulting in low jitter performance, typically 0.5pS rms in the 12 kHz to 20MHz band. Also a monolithic IC, which improves reliability and reduces cost, is hermitically sealed.

Performance Characteristics

Table 1. Electrical Performance, 5V option

Parameter	Symbol	Min	Typical	Maximum	Units
Frequency	f_O	0.012		125.000	MHz
Operating Supply Voltage [1]	V_{DD}	4.5		5.5	V
Absolute Maximum Supply Voltage		-0.7		7.0	V
Supply Current, Output Enabled	I_{DD}				mA
<1.5 MHz				7	
1.5 to 20 MHz				10	
20.01 to 50 MHz				30	
50.00 to 85 MHz				50	
85.01 to 125 MHz				60	
Supply Current, Out disabled	I_{DD}			30	uA
Output Logic Levels					
Output Logic High[2]	V_{OH}	0.9*V_{DD}			V
Output Logic Low[2]	V_{OL}			0.1*V_{DD}	V
Output Logic High Drive	I_{OH}	16			mA
Output Logic Low Drive	I_{OL}	16			mA
Output Rise/Fall Time[2]	t_R/t_F				ns
< 1.00 MHz				200	
1.0 to 20.00 MHz				8	
20.01 to 50.00 MHz				5	
50.01 to 125.00 MHz				2	
Duty Cycle[3] *(ordering option)*	SYM	45/55			%
Operating temperature (*ordering option*)		-10/70 or -40/85			°C
Stability[4] (*ordering option)*		±20, ±25, ±32, ±50, ±100			ppm
RMS Jitter, 12kHz to 20 MHz			0.5	1	ps
Period Jitter, RMS			2.5		ps
Output Enable/Disable[5]					V
Output Enabled		4.0			
Output Disabled				0.8	
Internal Enable Pull-Up resistor[5]			100		Kohm
Start-up time				10	ms

1. A 0.01uF and a 0.1uF capacitor should be located as close to the supply as possible (to ground) is recommended.
2. Figure 1 defines these parameters. Figure 2 illustrates the operating conditions under which these parameters are tested and specified.
3. Symmetry is measured defined as Vs, On Time/Period.
4. Includes calibration tolerance, operating temperature, supply voltage variations, aging and shock and vibration (not under operation).
5. Output will be enabled if enable/disable is left open.

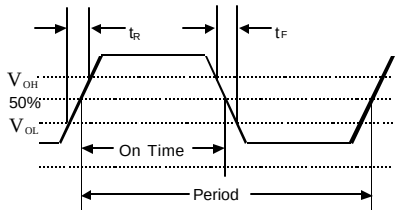


Figure 1. Output Waveform

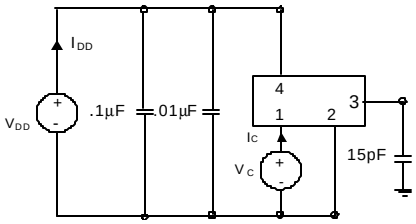


Figure 2. Typical Output Test Conditions (25±5°C)

Table 2. Electrical Performance, 3.3V option					
Parameter	**Symbol**	**Min**	**Typical**	**Maximum**	**Units**
Frequency	f_O	0.012		189.000	MHz
Operating Supply Voltage [1]	V_{DD}	2.97	3.3	3.63	V
Absolute Maximum Operating Voltage		-0.5		5.0	V
Supply Current, Output Enabled	I_{DD}				mA
< 1.500 MHz				5	
1.5 to 20 MHz				7	
20.01 to 50 MHz				20	
50.00 to 85 MHz				30	
85.01 to 189 MHz				50	
Supply Current, Output disabled	I_{DD}			30	uA
Output Logic Levels					
Output Logic High[2]	V_{OH}	0.9*V_{DD}			V
Output Logic Low[2]	V_{OL}			0.1*V_{DD}	V
Output Logic High Drive	I_{OH}	8			mA
Output Logic Low Drive	I_{OL}	8			mA
Output Rise/Fall Time[2]	t_R/t_F				ns
< 1.00 MHz				200	
1.00 to 20.00 MHz				6	
20.01 to 50.00 MHz				4	
50.01 to 90.00 MHz				3	
90.01 to 189.00 MHz				2	
Duty Cycle[3] *(ordering option)*	SYM	45/55			%
Operating temperature (*ordering option*)		-10/70 or –40/85			°C
Stability[4] (*ordering option)*		±20, ±25, ±32, ±50, ±100			ppm
RMS Jitter, 12kHz to 20 MHz			0.5	1	ps
RMS Jitter			2.5		ps
Output Enable/Disable[5]					V
Output Enabled		2.0			
Output Disabled				0.5	
Internal Enable Pull-Up resistor[5]			100		Kohm
Start-up time				10	ms

1. A 0.01uF and a 0.1uF capacitor should be located as close to the supply as possible (to ground) is recommended.
2. Figure 3 defines these parameters. Figure 4 illustrates the operating conditions under which these parameters are tested and specified. For Fo>90MHz, rise and fall time is measured 20 to 80%.
3. Symmetry is measured defined as Vs, On Time/Period.
4. Includes calibration tolerance, operating temperature, supply voltage variations, aging and shock and vibration (not under operation).
5. Output will be enabled if enable/disable is left open.

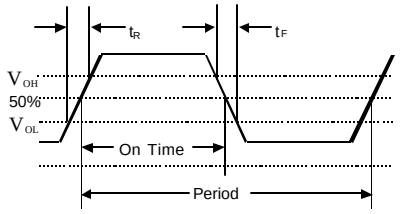


Figure 3. Output Waveform

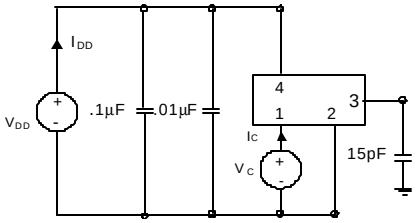


Figure 4. Typical Output Test Conditions (25±5°C)

Table 3. Electrical Performance, 2.5V option					
Parameter	**Symbol**	**Min**	**Typical**	**Maximum**	**Units**
Frequency	f_O	0.012		172.000	MHz
Operating Supply Voltage [1]	V_{DD}	2.25	2.5	2.75	V
Absolute Maximum Voltage		-0.5		5.0	V
Supply Current, Output Enabled	I_{DD}				mA
< 20 MHz				7.0	
20.01 to 50 MHz				15.0	
50.00 to 110 MHz				20.0	
110.1 to 172 MHz				30.0	
Supply Current, Out disabled	I_{DD}			30	uA
Output Logic Levels					
Output Logic High[2]	V_{OH}	0.9*V_{DD}			V
Output Logic Low[2]	V_{OL}			0.1*V_{DD}	V
Output Logic High Drive	I_{OH}	4			mA
Output Logic Low Drive	I_{OL}	4			mA
Output Logic High Drive[3]	I_{OH}	8			mA
Output Logic Low Drive[3]	I_{OL}	8			mA
Output Rise/Fall Time[2]	t_R/t_F				ns
<1.00 MHz				200	
1.00 to 20.00 MHz				10	
20.01 to 50.00 MHz				6	
50.01 to 90.00 MHz				3	
90.01 to 172.00 MHz				2	
Duty Cycle[4] *(ordering option)*	SYM	45/55			%
Operating temperature (*ordering option*)		-10/70 or –40/85			°C
Stability[5] (*ordering option)*		±20, ±25, ±32, ±50, ±100			ppm
RMS Jitter, 12kHz to 20 MHz			0.5	1	ps
RMS Jitter			2.5		ps
Output Enable/Disable[6]					V
Output Enabled		1.75			
Output Disabled				0.5	
Internal Enable Pull-Up resistor[6]			100		Kohm
Start-up time				10	ms

1. A 0.01uF and a 0.1uF capacitor should be located as close to the supply as possible (to ground) is recommended.
2. Figure 5 defines these parameters. Figure 6 illustrates the operating conditions under which these parameters are tested and specified.
3. Overtone designs, output frequencies>35MHz.
4. Symmetry is measured defined as Vs, On Time/Period.
5. Includes calibration tolerance, operating temperature, supply voltage variations, aging and shock and vibration (not under operation).
6. Output will be enabled if enable/disable is left open.

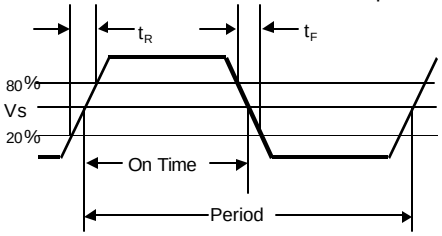


Figure 5. Output Waveform

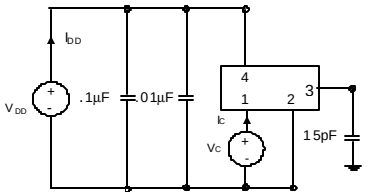


Figure 6. Typical Output Test Conditions (25±5°C)

Table 4. Electrical Performance, 1.8V option					
Parameter	**Symbol**	**Min**	**Typical**	**Maximum**	**Units**
Frequency	f_O	0.048		172.000	MHz
Operating Supply Voltage [1]	V_{DD}	1.71	1.8	1.89	V
Absolute Maximum Voltage		-0.5		3.6	V
Supply Current, Output Enabled	I_{DD}				mA
< 20 MHz				5	
20.01 to 70 MHz				15	
70.01 to 96 MHz				20	
96.01 to 125 MHz				25	
125.01 to 172 MHz				30	
Supply Current, Out disabled	I_{DD}			30	uA
Output Logic Levels					
Output Logic High [2]	V_{OH}	0.9*V_{DD}			V
Output Logic Low [2]	V_{OL}			0.1*V_{DD}	V
Output Logic High Drive	I_{OH}	2.8			mA
Output Logic Low Drive	I_{OL}	2.8			mA
Output Logic High Drive [3]	I_{OH}	8			mA
Output Logic Low Drive [3]	I_{OL}	8			mA
Output Rise/Fall Time [2]	t_R/t_F				ns
< 1.00 MHz				200	
1.000 to 20.00 MHz				4	
20.01 to 50.00 MHz				4	
50.00 to 90.00 MHz				3	
90.01 to 172.00 MHz				2	
Duty Cycle [4] (*ordering option*)	SYM	45/55			%
Operating temperature (*ordering option*)		-10/70 or –40/85			°C
Stability [5] (*ordering option)*		±20, ±25, ±32, ±50, ±100			ppm
RMS Jitter, 12kHz to 20 MHz			0.5		ps
RMS Jitter			2.2		ps
Output Enable/Disable [6]					V
Output Enabled		1.26			
Output Disabled				0.5	
Internal Enable Pull-Up resistor [6]			1		Mohm
Start-up time				10	ms

1. A 0.01uF and a 0.1uF capacitor should be located as close to the supply as possible (to ground) is recommended.
2. Figure 7 defines these parameters. Figure 8 illustrates the operating conditions under which these parameters are tested and specified.
3. Overtone designs, output frequencies>35MHz.
4. Symmetry is measured defined as Vs, On Time/Period.
5. Includes calibration tolerance, operating temperature, supply voltage variations, aging and shock and vibration (not under operation).
6. Output will be enabled if enable/disable is left open.

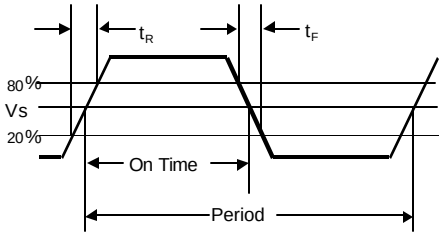


Figure 7. Output Waveform

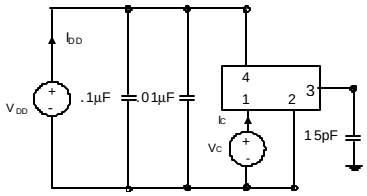


Figure 8. Typical Output Test Conditions (25±5°C)

Enable/Disable Functional Description

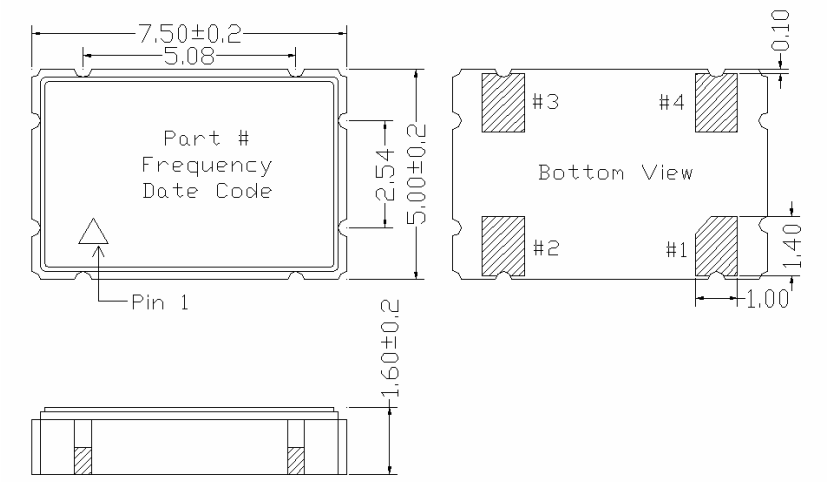
Under normal operation the Enable/Disable is left open or set to a logic high state. When the E/D is set to a logic low, the oscillator stops and the output is in a high impedance state. This helps reduce power consumption as well as facilitating board testing and troubleshooting.

TriState Functional Description

Under normal operation the Tristate is left open or set to a logic high state. When the Tri-State is set to a logic low, the oscillator remains active but the output buffer is in a high impedance state. This helps facilitate board testing and troubleshooting.

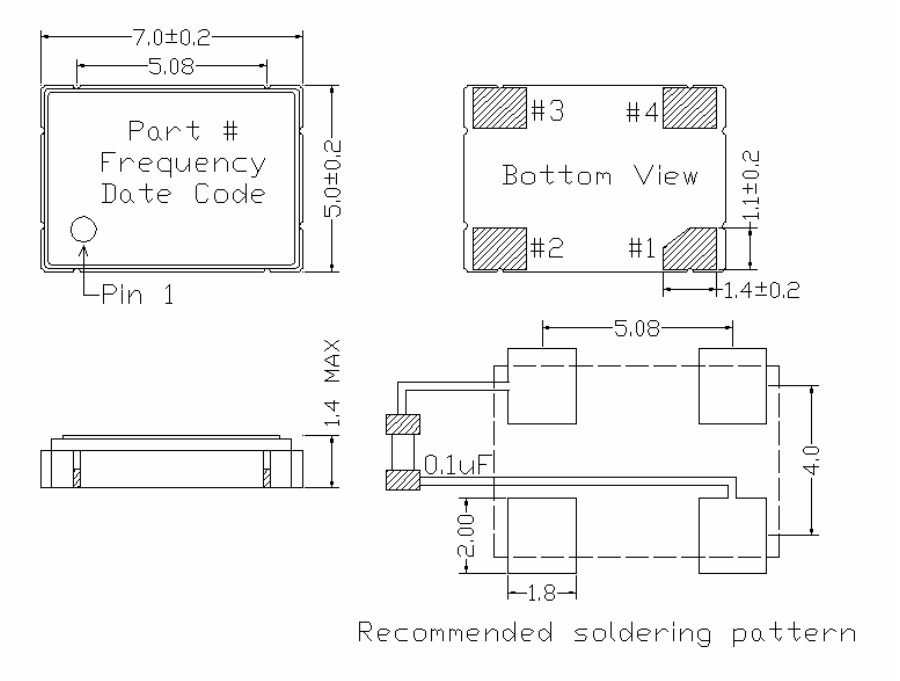
Outline Diagrams, Pad Layout and Pin Out

Pin #	Symbol	Function
1	E/D or NC	Tristate, Enable/Disable or NC
2	GND	Electrical and Case Ground
3	f_O	Output Frequency
4	V_{DD}	Supply Voltage



Contact Pads are gold over nickel

Figure 9, Package drawing

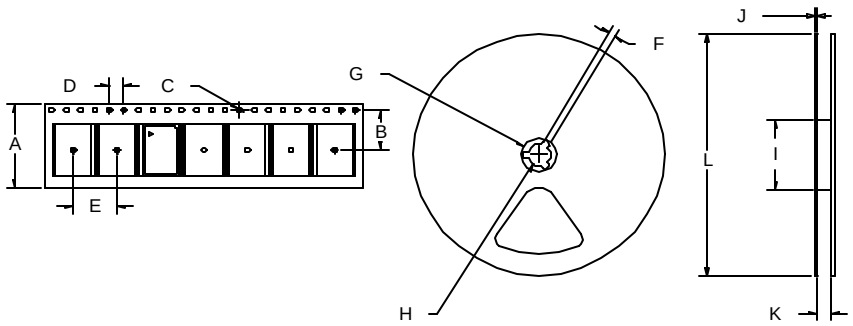


Contact Pads are gold over nickel

Figure 10, Alternate Package drawing

Tape and Reel

Table 5: Tape and Reel Dimensions (mm)



Tape Dimensions						Reel Dimensions							# Per
Product	A	B	C	D	E	F	G	H	I	J	K	L	Reel
VCC1	12	5.5	1.5	4	8	1.78	20.6	13	55	6	12.4	178	1000

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability.

Table 6. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Storage Temperature	Tstorage	-55/125	°C

Reliability

The VCC1 qualification tests have included:

Table 7. Environnemental Compliance

Parameter	Conditions
Mechanical Shock	MIL-STD-883 Method 2022
Mechanical Vibration	MIL-STD-883 Method 2007
Temperature Cycle	MIL-STD-883 Method 1010
Solderability	MIL-STD-883 Method 2003
Gross and Fine Leak	MIL-STD-883 Method 1014
Resistance to Solvents	MIL-STD-883 Method 2015

Handling Precautions

Although ESD protection circuitry has been designed into the the VCC1, proper precautions should be taken when handling and mounting. VI employs a Human Body Model and a Charged-Device Model (CDM) for ESD susceptibility testing and design protection evaluation. ESD thresholds are dependent on the circuit parameters used to define the model. Although no industry wide standard has been adopted for the CDM, a standard HBM of resistance = 1.5kohms and capacitance = 100pF is widely used and therefore can be used for comparison purposes.

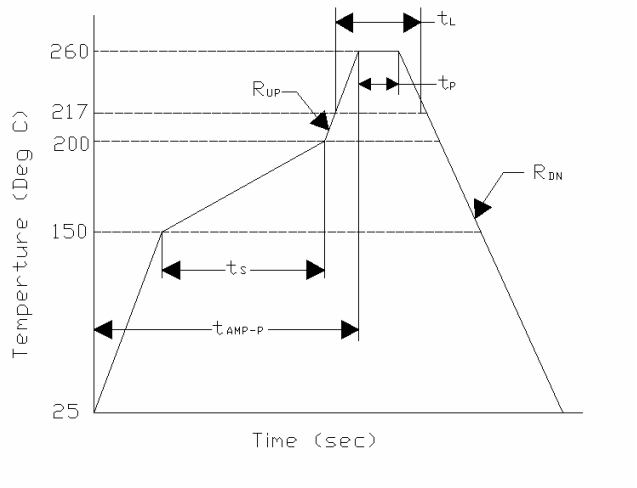
Table 8. ESD Ratings

Model	Minimum	Conditions
Human Body Model	1000	MIL-STD-883 Method 3115
Charged Device Model	1500	JESD 22-C101

Suggested IR profile

Devices are built using lead free epoxy and can also be subjected to standard lead free IR reflow conditions, Table 9 shows max temperatures and lower temperatures can also be used e.g. peak temperature of 220C.

Table 9. Reflow Profile (IPC/JEDEC J-STD-020B)		
Parameter	**Symbol**	**Value**
PreHeat Time	t_S	150 sec Min, 200 sec Max
Ramp Up	R_{UP}	3 °C/sec Max
Time Above 217 °C	t_L	60 sec Min, 150 sec Max
Time To Peak Temperature	t_{AMB-P}	480 sec Max
Time At 260 °C (max)	t_P	10 sec Max
Time At 240 °C (max)	t_{p2}	60 sec Max
Ramp Down	R_{DN}	6 °C/sec Max



Ordering Information

VCC1 - [B] [3] [B] - [125M00]

Product Family

Crystal Oscillator

Output Frequency

In MHZ

Voltage Options

A: +5.0 Vdc +/-10% , 15pF
B: +3.3 Vdc +/-10%, 15pF
C: +3.0 Vdc +/-10%, 15pF
E: +5.0 Vdc +/-10%, 50pF
F: +3.3Vdc +/-10%, 50pF
G: +2.5Vdc +/-10%, 15pF
H: +1.8Vdc +/-10%, 15pF

Electrical Options

3: Tristate, 45/55% Duty

The following codes are not recommended for new designs

0: No tristate, 40/60% Duty
1: Tristate, 40/60% Duty
2: No tristate, 45/55%Duty
5: Enable, 40/60% Duty
6: Enable, 45/55% Duty

Stability Options

A: ±100ppm, -10 to 70C
C: ±100ppm, -40 to 85C
B: ±50ppm, -10 to 70C
D: ±50ppm, -40 to 85C
K: ±32ppm, -10 to 70C
O: ±32ppm, -40 to 85C
E: ±25ppm, -10 to 70C
F: ±25ppm, -40 to 85C
G: ±20ppm, -10 to 70C

Note: Not all combinations are available. Tristate with a 45/55% is the most common Electrical code and is recommended for most applications.

For Additional Information, Please Contact:

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