MN1280, MN12801

CMOS LSIs for Supply Voltage Detection

Outline

The MN1280 and MN12801 generate a reset signal for initializing microcomputers and LSI systems at their power-on time, and a reset signal for preventing an abnormal system run at power fluctuation time.

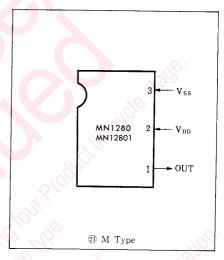
Features

- Generates a reset signal at power-on time until reaching a constant voltage.
- Generates a reset signal below a constant voltage at power-off time.
- Generates a reset signal when the supply voltage falls, and cancels it when the supply voltage is restored.
- Capable of detecting a battery service life.
- 3-pin adjustment-free device
- High-accuracy voltage detection
- Detected voltage value having hysteresis characteristic

Detected voltage at voltage rise time: V_{DH} , Detected voltage at voltage fall time: V_{DL} $V_{DH} - V_{DL} = 100$ to $300 \mathrm{mV}$

- Low power consumption: $10\mu A$ (typ.) at $V_{DD}=5V$
- Little detected voltage temperature change Temperature coefficient 1mv/°C(typ.)
- Open drain output buffer for MN12801

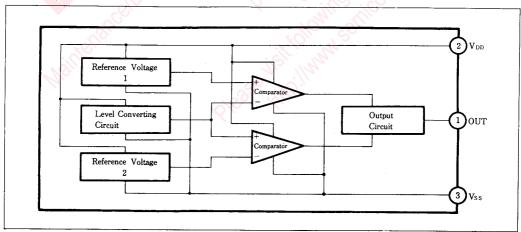
Pin Configuration



Pin Descriptions

Pin No.	Symbol	Description				
2	V _{DD}	Supply voltage pin				
3	Vss	Ground pin				
	OUT	Reset signal output pin. Low level at reset time. The "H" level is outputted when reset is cancelled.				

■ Block Diagram



■ V_{DL} Classifications(Detected Voltage at Supply Voltage Fall Time: V_{DL})

Class	L	M	N	P	Q	R	S	T	U
$V_{DL}(V)$	3.0~3.3	3.2~3.5	3.4~3.7	3.6~3.9	3.8~4.1	4.0~4.3	4.2~4.5	4.4~4.7	4.6~4.9

■ Absolute Maximum Ratings(V_{ss}=0 V, Ta=25°C)

Item	Symbol	Rating	Unit
Supply voltage	V _{DD}	7.0	V
OUtput voltage	Vo	$-0.3 - V_{DD} + 0.3$	V
Operating ambient temperature	Topr	$-20 \sim +70$	°C
Storage temperature	Tsig	-55~+125	°C

■ Operating Range(V_{SS}=0 V, Ta=25°C)

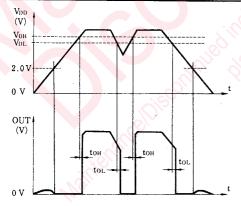
Item	Symbol	Condition	min.	typ.	max.	Unit
Supply voltage	V_{DD}	See Fig.2 and Fig.2	2.0		6.0	v

■ DC Electrical Characteristics(V_{SS}=0 V, Ta=-20 to +70°C)

Item	Symbol	Condition	min.	typ.	max.	Unit
Supply current	I_{DD}	V _{DD} =5 V at no-load output	(0)	10	30	μ A
Detected voltage hysteresis width	VDL	Ta=25°C. See Fig.1 and Fig.2	3.0		4.9	V
Detected voltage at supply voltage fall	ΔV_D	Ta=25°C. See Fig.1 and Fig.2	100	200	300	mV
Output voltage high level	Von	$I_{OH} = -40\mu A$	0.8V _{DD}		V _{DD}	V
Output voltage low level	Vol	$I_{OL}=0.7\text{mA}$ $V_{DD}=3V$	Vss		0.4	v

■ AC Electrical Characteristics

Item	Symbol	Condition	min.	typ.	max.	Unit
Reset cancel time	toн	See Fig.3	10	5	Ç	μs
Reset time	toL	See Fig.3	100	3		μs

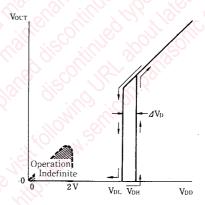


Note 1) When the supply voltage is less than 2 V, no output can be prescribed because operation is not assured.

Note 2) V_{DL}: Detected voltage at power fall time V_{DL}: Detected voltage at power rise time tou: Time for output(OUT) to reach the "H" level after the supply voltage rises to V_{DL}.

tol : Time for output(OUT) to reach the "L" level after the supply voltage falls to V_{DL}.

Fig. I Operation Chart



Note 1) When the supply voltage is less than 2 V, no output can be prescribed because operation is not assured.

Note 2) V_{DL} : Detected voltage at power fall time V_{DH} : Detected voltage at power rise time

Fig.2 I/O Characteristic Chart

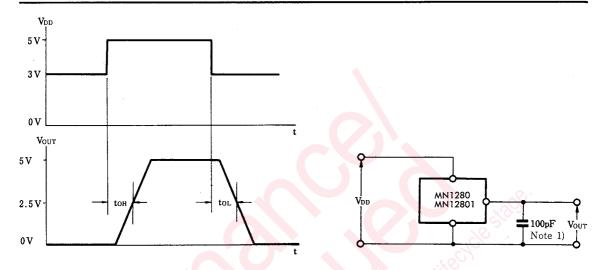


Fig.3 Output Characteristic Measurement Chart

Note 1) A capacitor capacitance of 100 pF is a value for mesurement. In actual use, increase it in accordance with need for a delay time.

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