AN3310K, AN3310S

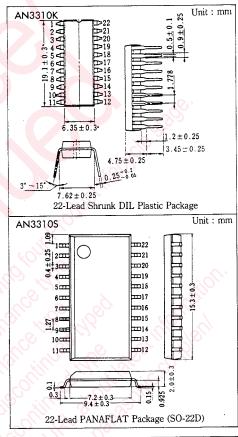
Head Amplifier Circuits for VTR (4-Head Type)

Outline

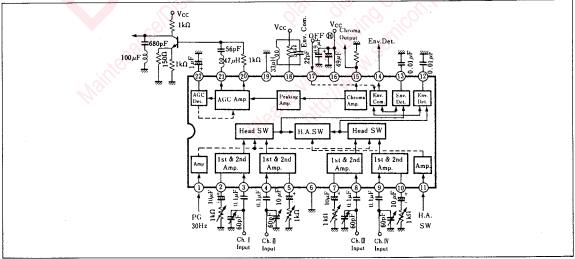
The AN3310K and the AN3310S are integrated circuits designed for head amplifier circuits for VTR (4-head type).

■ Features

- · Built-in enveloped comparing circuit
- · Built-in peaking amplifier circuit
- · Less noise voltage referred to input : 1 μ Vrms)
- · Supply voltage : Vcc=5V



Block Diagram



Pin

Pin No.	Pin Name	Pin No.	Pin Name	
1	Head SW Changeover	12	Ch. I, Il Side Envelope Detection	
2	Initial Stage Bias(Ch. I)	13	Ch. II, N Side Envelope Detection	
3	Initial Stage Input(Ch. I)	14	Envelope Comparative Output	
4	Initial Stage Input(Ch. II)	15	Chroma Output	
5	Initial Stage Bias(Ch. II)	16	Vcc	
6	Input Stage GND	17	Envelope Comparative Circuit Stop SW	
7	Initial Stage Bias(Ch. II)	18	Peaking Circuit Peak Constant	
8	Initial Stage Input(Ch. II)	19	Output Stage GND	
9	Initial Stage Input(Ch. N)	20	AGC Output	
10	Initial Stage Bias(Ch. N)	21	AGC Reverse Phase Output	
11	Head Amp. SW Changeover	22	AGC Control Signal Detection	

■ Absolute Maximum Ratings (Ta=25°C)

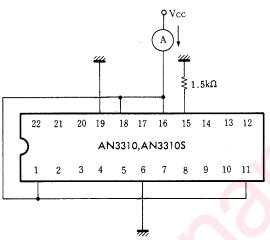
Item	Symbol	Rating	Unit
Supply Voltage	V _C	6.0	V
Power Dissipation(Ta=70℃)	P_{D}	250	mW
Operating Ambient Temperature	T_{opr}	-20~+70	°C
Storage Temperature	$T_{ m stg}$	-55~+150	℃

■ Electrical Characteristics (Ta=25°C)

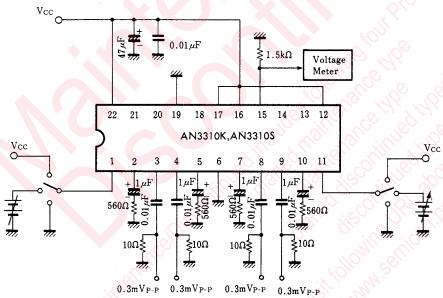
Item	Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Circuit Current	I ₁₆	1	V _{CC} =5V	16	2/,,	40	mA
Ch. I Gain	G ₃₋₁₅	2	V _{CC} =5V, f=1MHz	50.5		60.5	dB
Ch. I Gain	G ₄₋₁₅	2	V _{CC} =5V, f=1MHz	50.5		60.5	dΒ
Ch. II Gain	G ₈₋₁₅	2	V _{CC} =5V, f=1MHz	50.5		60.5	dΒ
Ch. N Gain	G ₉₋₁₅	2	V _{CC} =5V, f=1MHz	50.5		60.5	dB
AGC Output Amplitude	v_{20}	3	V _{CC} =5V, f=4MHz	100		190	mv_{P-P}
AGC Control Sensitivity	v_{20}	3	V _{CC} =5V, f=4MHz			3	dB
H.SW Changeover Sensitivity	S ₁	2	V _{CC} =5V			1	V
H.A.SW Changeover Sensitivity	S ₁₁	2	V _{CC} =5V			1	V
Noise voltage Referred to Input(1)	V _{ni3-15}	4	V _{CC} =5V, 1MHz BPF			1	$\mu V_{ m rms}$
Noise voltage Referred to Input(1)	V _{ni4-15}	4	V _{CC} =5V, 1MHz BPF			1	μV_{rms}
Noise voltage Referred to Input(II)	V _{ni8-15}	4	V _{CC} =5V, 1MHz BPF			1	μV_{rms}
Noise voltage Referred to Input(N)	V _{ni9-15}	4	V _{CC} =5V, 1MHz BPF			1	μV_{rms}
Envelope Comparative Output Amplitude	v_{14}	5	V _{CC} =5V	4.3			V_{P-P}
Envelope Comparative Output Stop Sensitivity	S ₁₇	5	V _{CC} =5V			1.2	V

Note: Operating Supply Voltage Range: V_{CC(opr)})=4.5~5.5V

Test Circuit 1 (I₁₆)

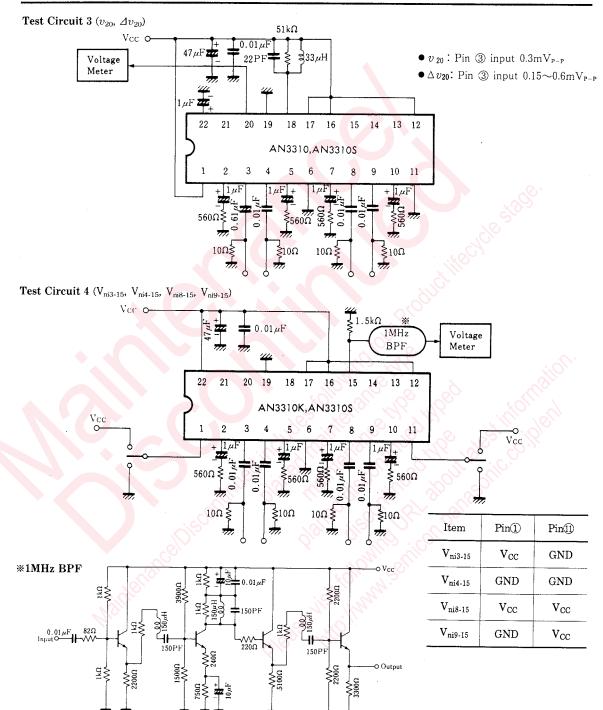


Test Circuit 2 (G_{3-15} , G_{4-15} , G_{8-15} , G_{9-15} , S_1 , S_{11})



Item	①Pin	①Pin	Input Pin
G _{3 · 15}	V_{CC}	GND	3
G _{4 · 15}	GND	GND	4
G ₈₋₁₅	v_{cc}	v_{cc}	8
G _{9 15}	GND	v_{cc}	9

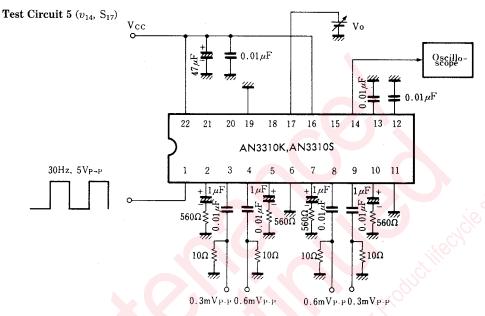
- \cdot S₁, S₁₁: Pin 4 0.3mV_{P-P} input (fin=1MHz)
- · S₁: Decreasing the electric potential of Pin ① from Vcc, measure the electric potential of Pin ① when Pin ⑤ output appears.
- · Su: Decreasing the electric potential of Pin
 from Vcc, measure the electric potential
 of Pin when Pin
 output appears.



O Notes for Handling

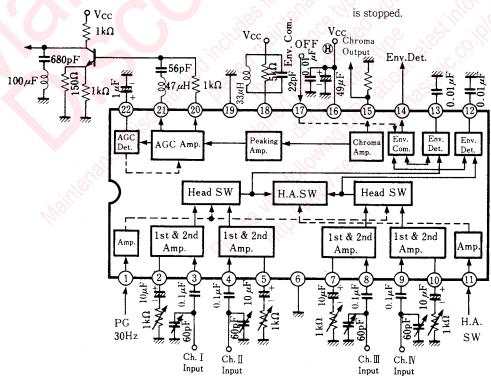
Since deterioration or destroy of characteristics may occur due to flow of overcurrent caused by the wrong insertion careful attention should be taken to handling.

Application Circuit



 $V_{14}: V_0 = 0V$

S17: Increasing the electric potential of
Vo from 0V, measure the electric
potential of Vo when Pin (4) output



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