

MITSUBISHI MICROCOMPUTERS

M37102M8-XXXSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER

DESCRIPTION

The M37102M8-XXXSP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 64-pin shrink plastic molded DIP. This single-chip microcomputer is useful for the high-tech channel selection system for TVs and VCRs.

In addition to their simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

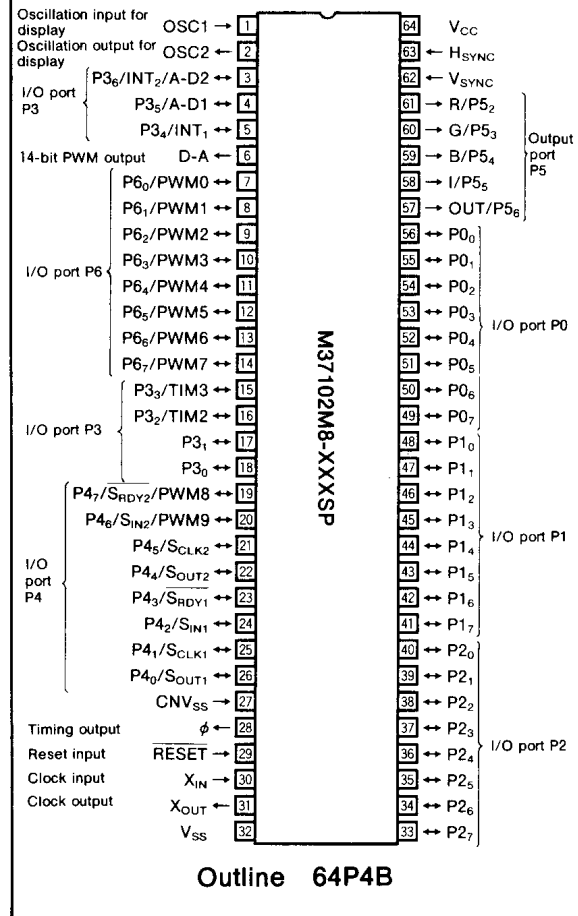
FEATURES

- Number of basic instructions..... 69
- Memory size ROM 16384 bytes
RAM 320 bytes
- Instruction execution time
..... 1 μ s (minimum instructions at 4MHz frequency)
- Single power supply 5V \pm 10%
- Power dissipation
normal operation mode (at 4MHz frequency)
..... 110mW (V_{CC} =5.5V, CRT display)
- Subroutine nesting 96 levels (Max.)
- Interrupt 13types, 13vectors
- 8-bit timer 4
- Programmable I/O ports
(Ports P0, P1, P2, P3, P4, P6) 47
- Output port (Port P5) 5
- Serial I/O (8-bit) 2
- PWM function 14-bit \times 1
8-bit \times 10
- A-D converter (4-bit resolution) 2 channels
- 72-character on screen display function
Number of character 24 characters \times 3 lines
Kinds of character 126

APPLICATION

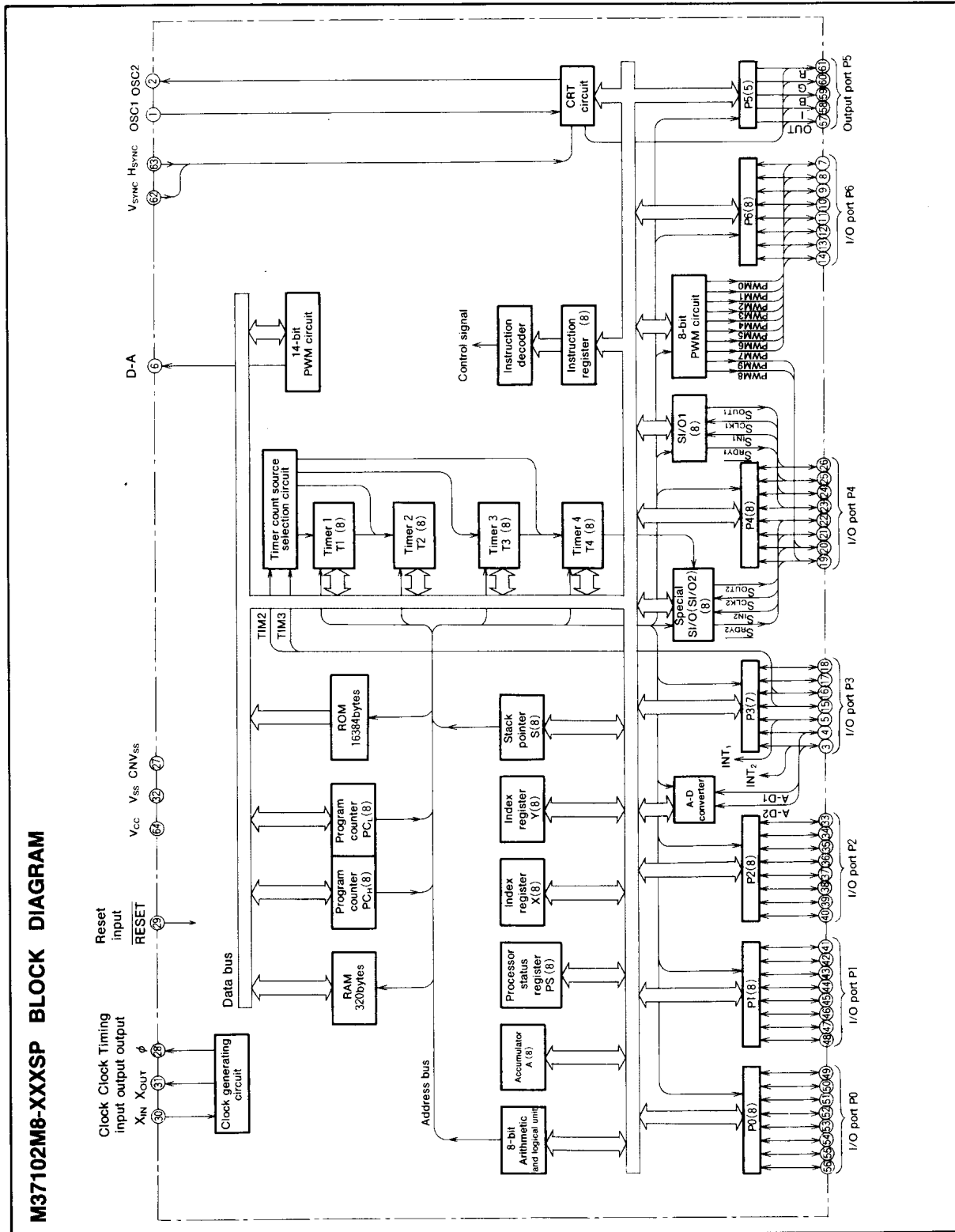
TV, VCR

PIN CONFIGURATION (TOP VIEW)



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FUNCTIONS OF M37102M8-XXXSP

Parameter		Functions
Number of basic instructions		69
Instruction execution time		1 μ s (minimum instructions, at 4MHz frequency)
Clock frequency		4MHz
Memory size	ROM	16384bytes
	RAM	320bytes
Input/Output ports	P0, P1, P2	I/O
	P3 ₀ , P3 ₁	I/O
	P3 ₂ ~P3 ₆	I/O
	P4	I/O
	P5	Output
	P6	I/O
Serial I/O		8-bit \times 2 (Special serial I/O (8-bit) \times 1)
Timers		8-bit timer \times 4
Subroutine nesting		96levels (max.)
Interrupt		Two external interrupts, nine internal interrupts, one software interrupt
Clock generating circuit		Two built-in circuits (externally connected ceramic or quartz crystal oscillator)
Supply voltage		5V \pm 10%
Power dissipation	at CRT display ON	110mW (clock frequency X_{IN} =4MHz, V_{CC} =5.5V, Typ.)
	at CRT display OFF	55mW (clock frequency X_{IN} =4MHz, V_{CC} =5.5V, Typ.)
	at stop mode	1.65mW (Max.)
Input/Output characteristics	Input/Output voltage	5V (Port P4 ₆ , P4 ₇ , P6 ₀ ~P6 ₇)
	Output current	10mA (Port P2 ₄ ~P2 ₇)
Operating temperature range		-10~70°C
Device structure		CMOS silicon gate process
Package		64-pin shrink plastic molded DIP
CRT display function	Number of character	24 characters \times 3 lines
	Kinds of character	126 (12 \times 16 dots)

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PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V _{CC} , V _{SS}	Supply voltage		Power supply inputs 5V±10% to V _{CC} , and 0V to V _{SS} .
CNV _{SS}	CNV _{SS}		This is connected to V _{SS} .
$\overline{\text{RESET}}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for more than 2 μ s (under normal V _{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X _{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X _{IN} and X _{OUT} pins. If an external clock is used, the clock source should be connected the X _{IN} pin and the X _{OUT} pin should be left open.
X _{OUT}	Clock output	Output	
ϕ	Timing output	Output	This is the timing output pin.
P0 ₀ ~P0 ₇	I/O port P0	I/O	Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is CMOS output.
P1 ₀ ~P1 ₇	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0.
P2 ₀ ~P2 ₇	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0.
P3 ₀ ~P3 ₆	I/O port P3	I/O	Port P3 is an 7-bit I/O port and has basically the same functions as port P0, but the output structure of P3 ₀ , P3 ₁ is CMOS output and the output structure of P3 ₂ ~P3 ₆ is N-channel open drain. P3 ₂ , P3 ₃ are in common with external clock input pins of timer 1 and 2. P3 ₄ , P3 ₅ are in common with external interrupt input pins INT ₁ and INT ₂ . P3 ₅ , P3 ₆ are in common with analog input pins of A-D converter (A-D1, A-D2).
P4 ₀ ~P4 ₇	I/O port P4	I/O	Port P4 is an 8-bit I/O port and has basically the same functions as port P0, but the output structure is N-channel open drain. When serial I/O1 is used, P4 ₀ , P4 ₁ , P4 ₂ and P4 ₃ work as S _{OUT1} , S _{CLK1} , S _{IN1} and $\overline{\text{SRDY1}}$ pins, respectively. When serial I/O2 is used, P4 ₄ , P4 ₅ , P4 ₆ and P4 ₇ work as S _{OUT2} , S _{CLK2} , S _{IN2} and $\overline{\text{SRDY2}}$ pins, respectively. Also P4 ₆ , P4 ₇ are in common with PWM output pins of PWM 8 and 9.
P6 ₀ ~P6 ₇	I/O port P6	I/O	Port P6 is an 8-bit I/O port and has basically the same functions as port P0, but the output structure is N-channel open drain. This port is in common with PWM output pins PWM0~PWM7.
OSC1, OSC2	Clock input for CRT display Clock output for CRT display	Input Output	This is the I/O pins of the clock generating circuit for the CRT display function.
H _{SYNC}	H _{SYNC} input	Input	This is the horizontal synchronizing signal input for CRT display.
V _{SYNC}	V _{SYNC} input	Input	This is the vertical synchronizing signal input for CRT display.
R, G, B, I, OUT	CRT output	Output	This is an 5-bit output pin for CRT display. The output structure is CMOS output. This is in common with port P5 ₂ ~P5 ₆ .
D-A	DA Output	Output	This is a output pin for 14-bit PWM.

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BASIC FUNCTION BLOCKS

MEMORY

A memory map for the M37102M8-XXXSP is shown in Figure 1. Addresses $C000_{16}$ to $FFFF_{16}$ are assigned to the built-in ROM area which consists of 16384 bytes.

Addresses $FF00_{16}$ to $FFFF_{16}$ are a special address area (special page). By using the special page addressing mode of the JSR instruction, subroutines addressed on this page can be called with only 2 bytes. Addresses $FFDE_{16}$, $FFDF_{16}$ and $FFE8_{16}$ to $FFFF_{16}$ are vector addresses used

for the reset and interrupts (see interrupt chapter). Addresses 0000_{16} to $00FF_{16}$ are the zero page address area. By using the zero page addressing mode, this area can also be accessed with 2 bytes. The use of these addressing methods will greatly reduce the object size required. The RAM, I/O port, timer, etc., are assigned to this area.

Addresses 0000_{16} to $00BF_{16}$ and 0100_{16} to $017F_{16}$ are assigned to the built-in RAM and consist of 320 bytes of static RAM. In addition to data storage, this RAM except the area in the page 1 is used for the stack during subroutine calls and interrupts.

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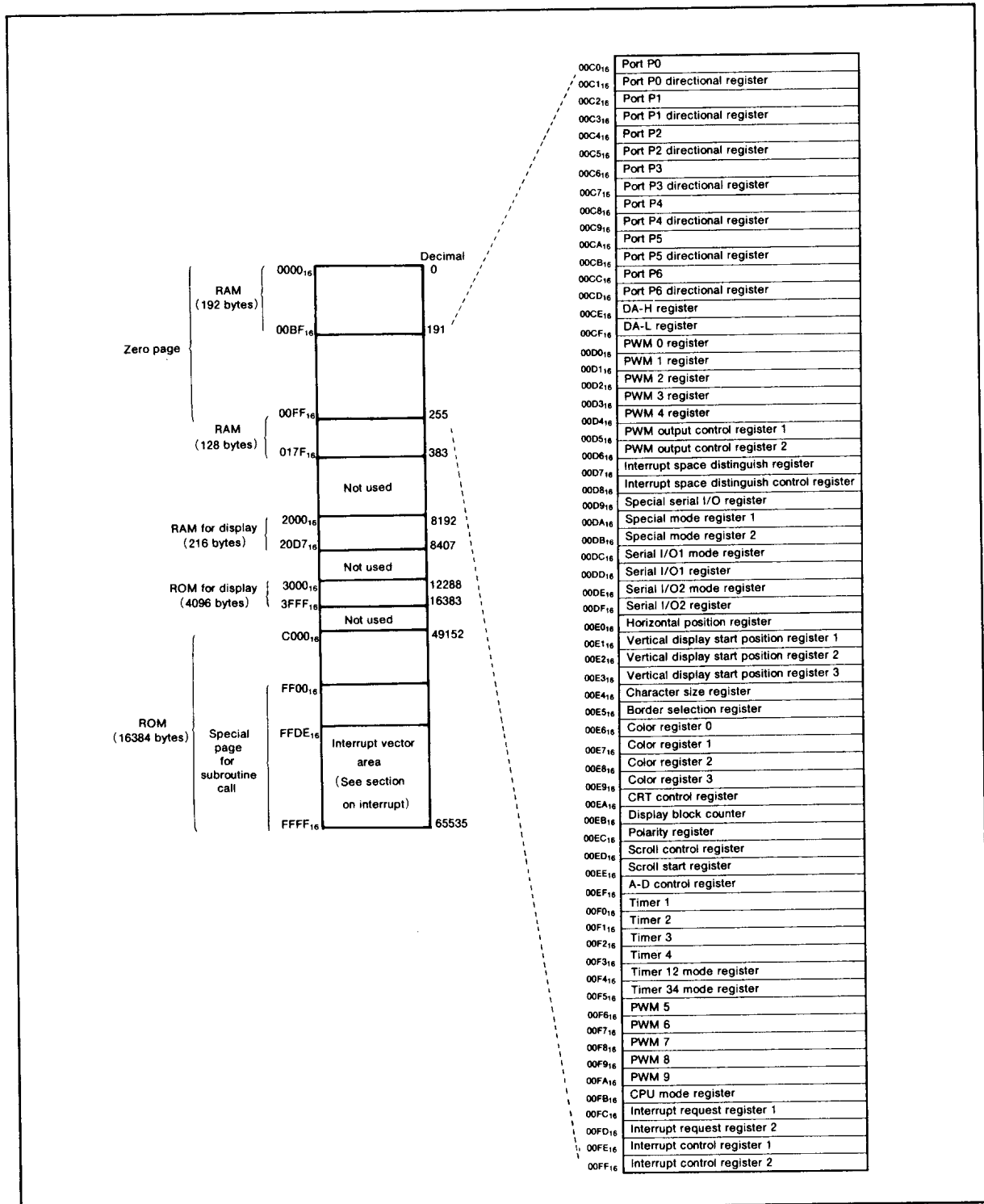


Fig. 1 Memory map

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CENTRAL PROCESSING UNIT (CPU)

The CPU consists of 6 registers and is shown in Figure 3.

ACCUMULATOR (A)

The 8-bit accumulator (A) is the main register of the micro-computer. Data operations such as data transfer, Input/Output, etc., are executed mainly through accumulator.

INDEX REGISTER X (X)

The index register X is an 8-bit register.

In the index addressing mode, the value of the OPERAND added to the contents of the register X, specifies the real address. When the T flag in the processor status register is set to "1", the index register X itself becomes the address for the second OPERAND.

INDEX REGISTER Y (Y)

The index register Y is an 8-bit register.

In the index addressing mode, the value of the OPERAND added to the contents of the register Y specifies the real address.

STACK POINTER (S)

The stack pointer (S) is an 8-bit register. It is used during subroutine calls and interrupts.

When there is an interrupts, the high-order contents of the program counter is pushed into the address formed by setting the high-order eight bits to 00₁₆ or 01₁₆ and the low-order eight bits to the content of the stack pointer. Next the stack pointer is decremented by one and the low-order content of the program counter is pushed into the address formed by setting the high-order eight bits to 00₁₆ or 01₁₆ and the low-order eight bits to the content of the stack pointer. Then the stack pointer is again decremented by one, the content of the processor status register is pushed into the address formed by setting the high-order eight bits to 00₁₆ or 01₁₆ and the low-order eight bits to the content of the stack pointer, and then the stack pointer is decremented by one once more. Whether to set 00₁₆ or 01₁₆ in the high-order eight bits is determined by bit 2 at address 00FB₁₆. The high-order eight bits are set to 00₁₆ if bit 2 at address 00FB₁₆ is "0" and to 01₁₆ if it is "1". At reset, it is set to "0", then can be changed by program.

The push operation described above is performed automatically when an interrupt occurs. The RTI instruction is used to return from an interrupt routine.

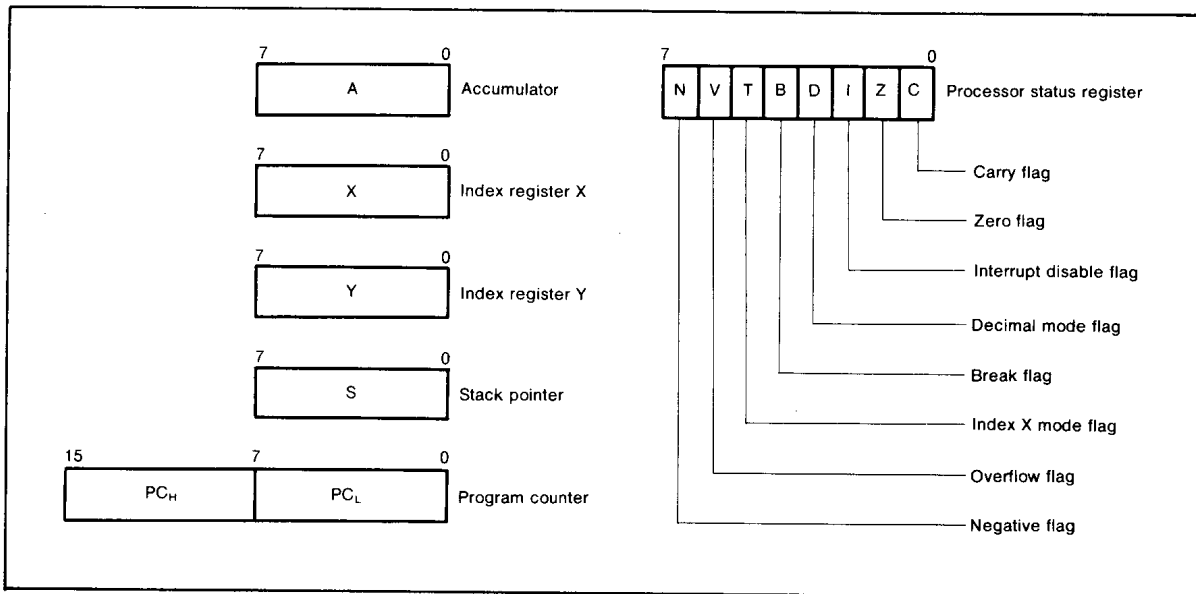


Fig. 2 Register structure

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When an RTI instruction is executed, control is returned by reversing the above operation while incrementing the stack pointer by one. The PHA instruction is used to push the accumulator because it is not saved automatically. When the PHA instruction is executed, the content of the accumulator is pushed into the address formed by setting the high-order eight bits to 00₁₆ or 01₁₆ and the low-order eight bits to the content of the stack pointer. Then the content of the stack pointer is decremented by one. The PLA instruction is used to restore the accumulator. When the PLA instruction is executed, the stack pointer is incremented by one and the content of the address formed by setting the high-order eight bits to 00₁₆ or 01₁₆ and the low-order eight bits to the content of the stack pointer is stored in the accumulator. The processor status register is pushed and restored in the same manner with the PHP and PLP instructions. With subroutine calls, only the program counter is pushed. Therefore, registers that must be preserved must be pushed by the program. Use the RTS instruction to return from a subroutine.

PROGRAM COUNTER (PC)

The 16-bit program counter consists of two 8-bit registers PC_H and PC_L. The program counter is used to indicate the address of the next instruction to be executed.

PROCESSOR STATUS REGISTER (PS)

The processor status register is composed entirely of flags used to indicate the condition of the processor immediately after an operation. Branch operations can be performed by testing the Carry flag (C), Zero flag (Z), Overflow flag (V) or the Negative flag (N). Each bit of the register is explained below.

1. Carry flag (C)

The carry flag contains the carry or borrow generated by the Arithmetic and Logical operation Unit (ALU) immediately after an operation. It also changed by the shift and rotate instructions. The set carry (SEC) and clear carry (CLC) instructions allow direct access for setting and clearing this flag.

2. Zero flag (Z)

This flag is used to indicate if the immediate operation generated a zero result or not. If the result is zero, the zero flag will be set to "1". If the result is not zero, the zero flag will be set to "0".

3. Interrupt disable flag (I)

This flag is used to disable all interrupts. This is accomplished by setting the flag to "1". When an interrupt, this flag is automatically set to "1" to prevent other interrupts from interfering until the current interrupt is completed. The SEI and CLI instructions are used to set and clear this flag, respectively.

4. Decimal mode flag (D)

The decimal mode flag is used to define whether addition and subtraction are executed in binary or decimal. If the decimal mode flag is set to "1", the operations are executed in decimal, if the flag is set to "0", the operations are executed in binary. Decimal correction is automatically executed. The SED and CLD instructions are used to set and clear this flag, respectively.

5. Break Flag (B)

The operation of a BRK instruction is similar to an interrupt. The BRK instruction is a non-maskable software interrupt that is used during program debugging. The break flag can be checked only by checking the content of the processor status register (PS) saved during an interrupt. The content of the processor status register (PS) is saved after setting flag B to "1" when the BRK instruction is used as an interrupt. It is cleared to "0" for other interrupts.

6. Index X mode flag (T)

When the T flag is "1", operations between memories are executed directly without passing through the accumulator. Operations between memories involving the accumulator are executed when the T flag is "0" (i.e., operation results between memories 1 and 2 are stored in the accumulator). The address of memory 1 is specified by the contents of the index register X, and that of memory 2 is specified by the normal addressing mode. The SET and CLT instructions are used to set and clear the index X mode flag, respectively.

7. Overflow flag (V)

The overflow flag functions when one byte is added or subtracted as a signed binary number. When the result exceeds +127 or -128, the overflow flag is set to "1". When the BIT instruction is executed, bit 6 of the memory location is input to the overflow flag. The overflow flag is clear by the CLV instruction and there is no set instruction.

8. Negative flag (N)

The negative flag is set whenever the result of a data transfer or operation is negative (bit 7 is set to "1"). Whenever the BIT instruction is executed, bit 7 of the memory location is input to the negative flag. There are no instructions for directly setting or clearing the negative flag.

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INTERRUPTS

Interrupts can be caused by 12 different events consisting of three external, eight internal, and one software events.

Interrupts are vectored interrupts with priorities shown in Table 1. Reset is also included in the table because its operation is similar to an interrupt.

When an interrupt is accepted, the registers are pushed as described in the stack pointer (S) section above, interrupt inhibit flag I is set, and the program jumps to the address specified in the vector table. The interrupt request flag is cleared automatically. The reset and BRK instruction interrupt can never be inhibited. Other interrupts are disabled when the interrupt inhibit flag is set.

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit. The interrupt request bits are in interrupt request registers 1 and 2 and the interrupt enable bits are in interrupt control registers 1 and 2. Figure 3 shows the structure of the interrupt request registers 1 and 2 and interrupt control registers 1 and 2.

Interrupts other than the BRK instruction interrupt and reset are accepted when the interrupt enable bit is "1", interrupt request bit is "1", and the interrupt inhibit bit is "0". The interrupt request bit can be reset with a program, but not set. The interrupt enable bit can be set and reset with a program.

Reset is treated as a non-maskable interrupt with the highest priority. Figure 4 shows interrupts control.

Table 1. Interrupt vector address and priority.

Event	Priority	Vector addresses	Remarks
RESET	1	FFFF ₁₆ , FFFE ₁₆	Non-maskable
CRT interrupt	2	FFFD ₁₆ , FFFC ₁₆	
INT ₂ interrupt	3	FFFB ₁₆ , FFFA ₁₆	
INT ₁ interrupt	4	FFF9 ₁₆ , FFF8 ₁₆	
Serial I/O 2 interrupt	5	FFF7 ₁₆ , FFF6 ₁₆	
Timer 4 interrupt	6	FFF5 ₁₆ , FFF4 ₁₆	
1 ms interrupt	7	FFF3 ₁₆ , FFF2 ₁₆	
V _{SYNC} interrupt	8	FFF1 ₁₆ , FFF0 ₁₆	
Timer 3 interrupt	9	FFEF ₁₆ , FFEE ₁₆	
Timer 2 interrupt	10	FFED ₁₆ , FFEC ₁₆	
Timer 1 interrupt	11	FFEB ₁₆ , FFEA ₁₆	
Serial I/O 1 interrupt	12	FFE9 ₁₆ , FFE8 ₁₆	
BRK instruction interrupt	13	FFDF ₁₆ , FFDE ₁₆	Non-maskable software interrupt

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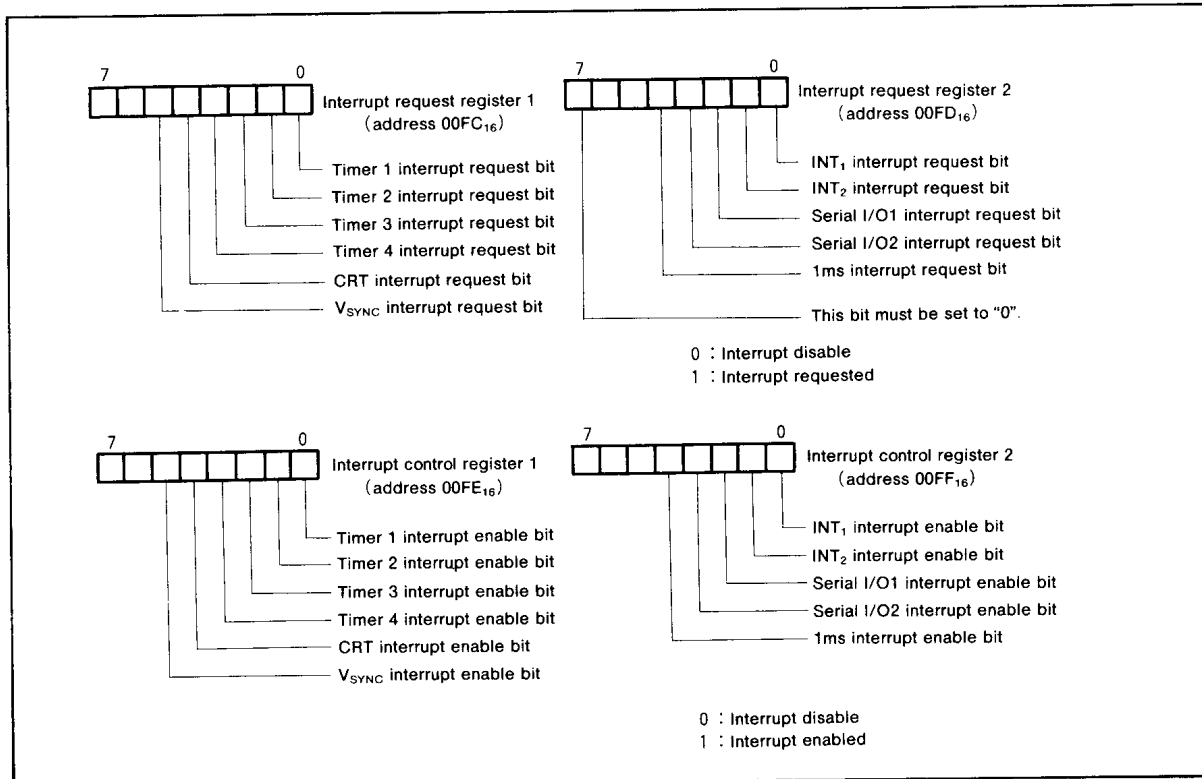


Fig. 3 Structure of registers related to interrupt

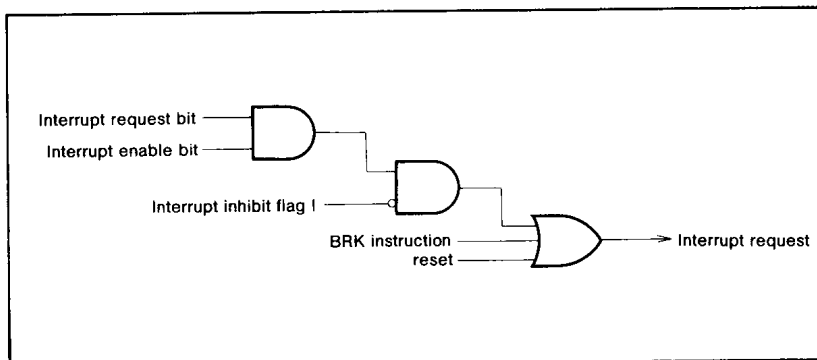


Fig. 4 Interrupt control

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TIMER

The M37102M8-XXXSP has four timers; timer 1, timer 2, timer 3 and timer 4.

A block diagram of timer 1 through 4 is shown in Figure 6.

The count source for timer 1 through 4 can be selected by using bit 0, 1, 4 of timer 12 mode register and timer 34 mode register (address $00F4_{16}$, $00F5_{16}$), as shown in Figure 5.

All of the timers are down count timers and have 8-bit latches. When a timer reaches " FF_{16} " and the next count pulse is input to a timer, a value which is subtracted 1 from the contents of the reload latch are loaded into the timer. The division ratio of the timer is $1/(n+1)$, where n is the contents of timer latch. The timer interrupt request bit is set at the next count pulse after the timer reaches " FF_{16} ".

The starting and stopping of the timer is controlled by bit 2, 3 of timer 12 mode register and timer 34 mode register.

At a reset or stop mode, FF_{16} is automatically set in timer 3 and 07_{16} in timer 4 and timer 3 and the clock ($f(X_{IN})$ divided by 16) are connected in series.

When restarting oscillation or canceling a reset, the internal clock is not supplied to the CPU until timer 4 overflows.

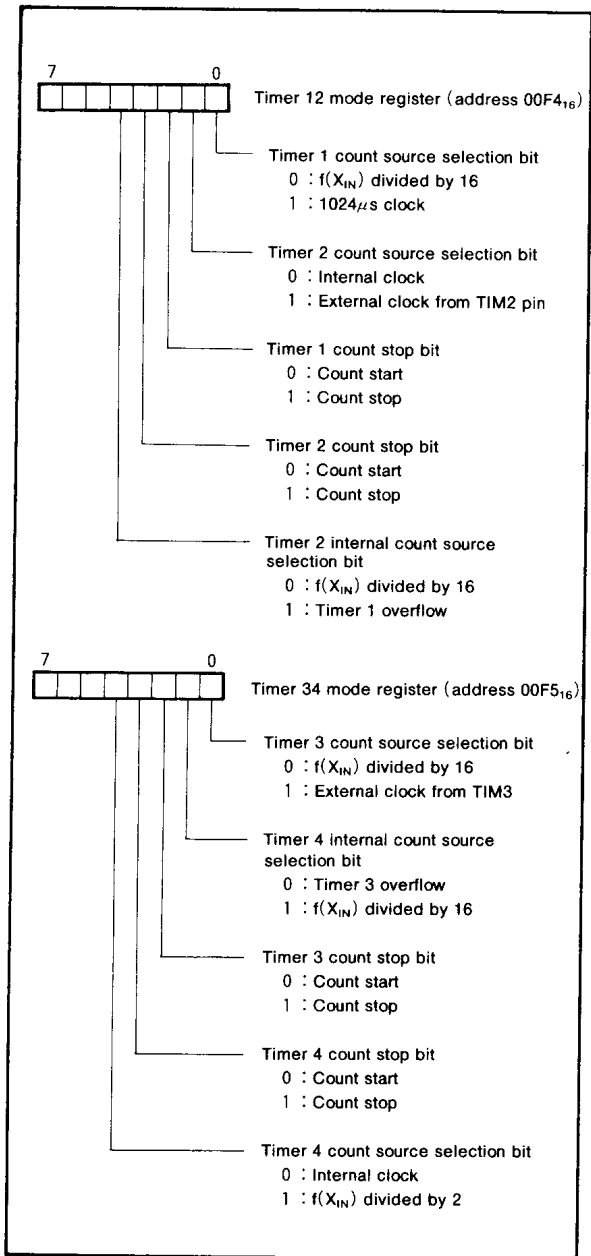


Fig. 5 Structure of timer 12 mode register and timer 34 mode register

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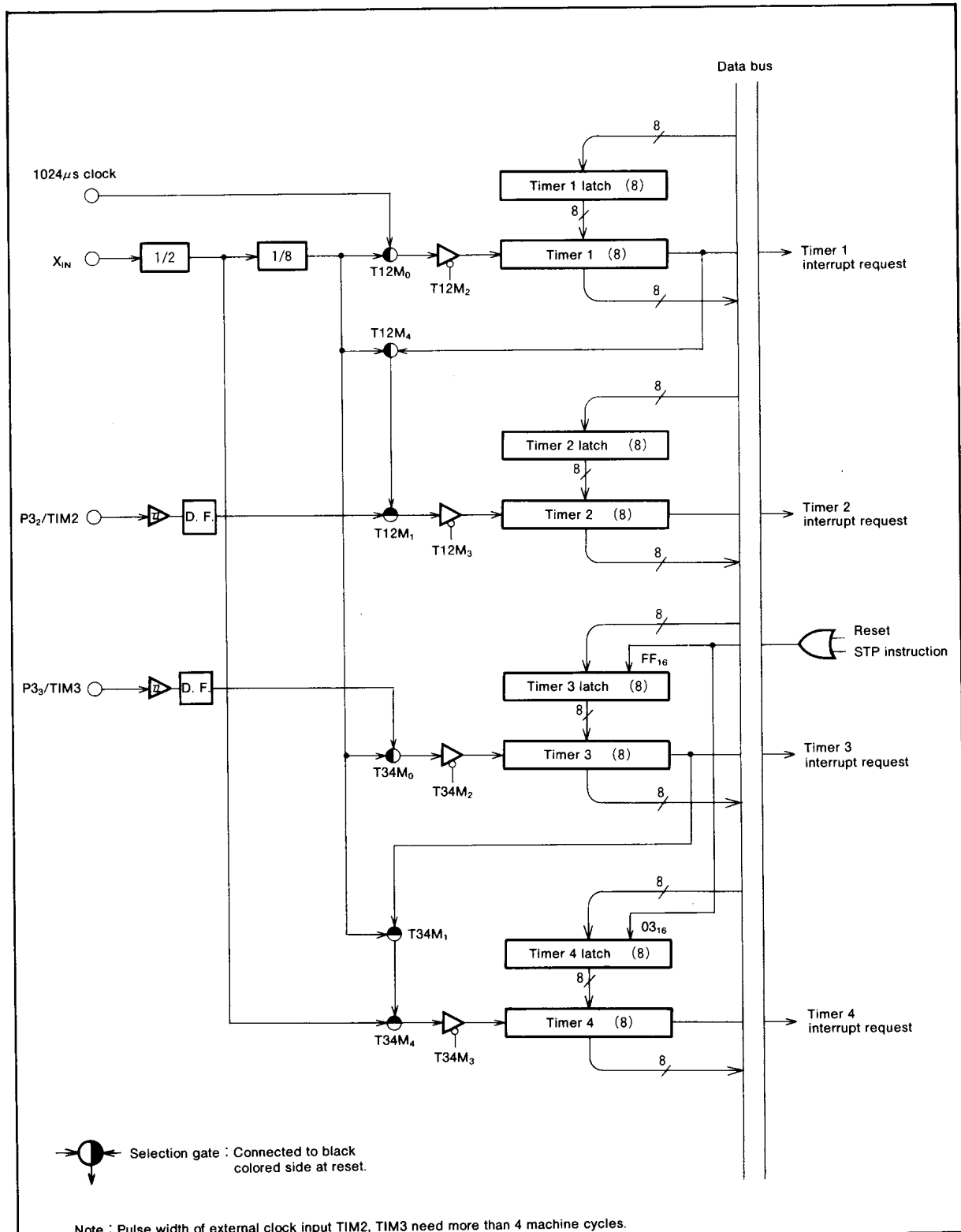


Fig. 6 Block diagram of timer 1, timer 2, timer 3 and timer 4

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SERIAL I/O

M37102M8-XXXSP has two serial I/O (serial I/O 1, serial I/O 2). Serial I/O 1 has the same function as serial I/O 2.

A block diagram of the serial I/O is shown in Figure 7.

In the serial I/O mode the receive ready signal ($\overline{S_{RDYi}}$), synchronous input/output clock (CLK_i), and the serial I/O pins (S_{OUTi} , S_{INi}) are used as port P4. The serial I/O_i mode registers (address 00DC₁₆, 00DE₁₆) are 8-bit registers. Bits 0, 1 and 2 of these registers are used to select a synchronous clock source.

Bit 3 and 4 decide whether parts of P4 will be used as a serial I/O or not.

To use P4₂ or P4₆ as a serial input, set the directional register bit which corresponds to P4₂ or P4₆ to "0". For more information on the directional register, refer to the I/O pin section.

Also to use internal clock of serial I/O 2, bit 1 of special mode register 1 (address 00DA₁₆) needs to be set to "1". The serial I/O function is discussed below. The function of the serial I/O differs depending on the clock source; external clock or internal clock.

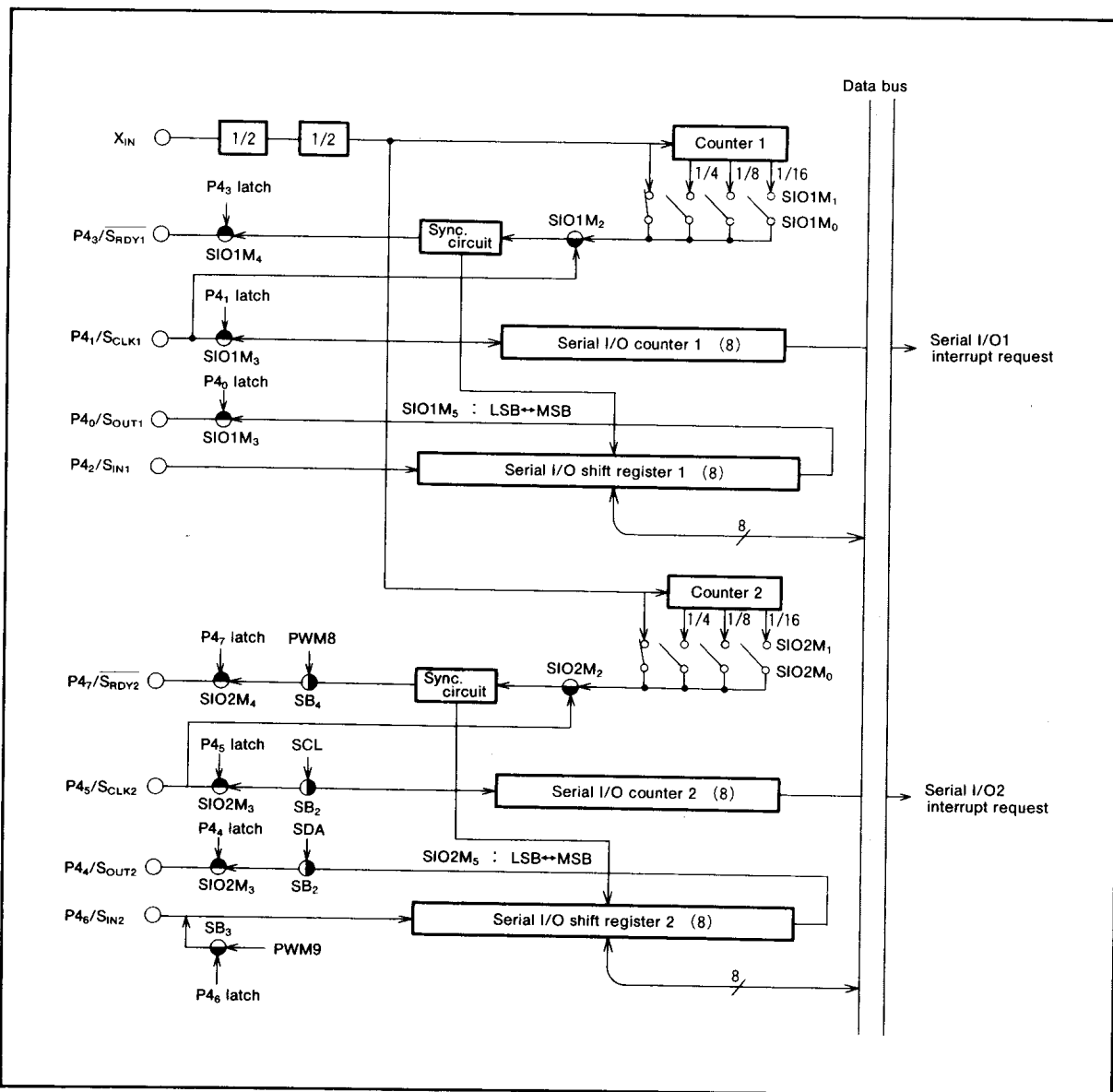


Fig. 7 Block diagram of serial I/O

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Internal clock — The \overline{SRDY}_i signal becomes "H" during transmission or while dummy data is stored in the serial I/O_i register (address 00DD₁₆, 00DF₁₆). After the falling edge of the write signal, the \overline{SRDY}_i signal becomes low signaling that the M37102M8-XXXSP is ready to receive the external serial data. The \overline{SRDY}_i signal goes "H" at the next falling edge of the transfer clock. The serial I/O_i counter is set to 7 when data is stored in the serial I/O_i register. At each falling edge of the transfer clock, serial data is output to S_{OUT*i*}. During the rising edge of this clock, data can be input from S_{IN*i*} and the data in the serial I/O_i register will be shifted 1 bit.

Transfer direction can be selected by bit 5 of serial I/O_i mode register. After the transfer clock has counted 8 times, the serial I/O_i register will be empty and the transfer clock will remain at a high level. At this time the interrupt request

bit will be set.

External clock- If an external clock is used, the interrupt request will be sent after the transfer clock has counted 8 times but transfer clock will not stop.

Due to this reason, the external clock must be controlled from the outside. The external clock should not exceed 500kHz at a duty cycle of 50%. The timing diagram is shown in Figure 8. When using an external clock for transfer, the external clock must be held at "H" level when the serial I/O_i counter is initialized. When switching between the internal clock and external clock, the switching must not be performed during transfer. Also, the serial I/O counter must be initialized after switching.

An example of communication between two M37102M8-XXXSPs is shown in Figure 9.

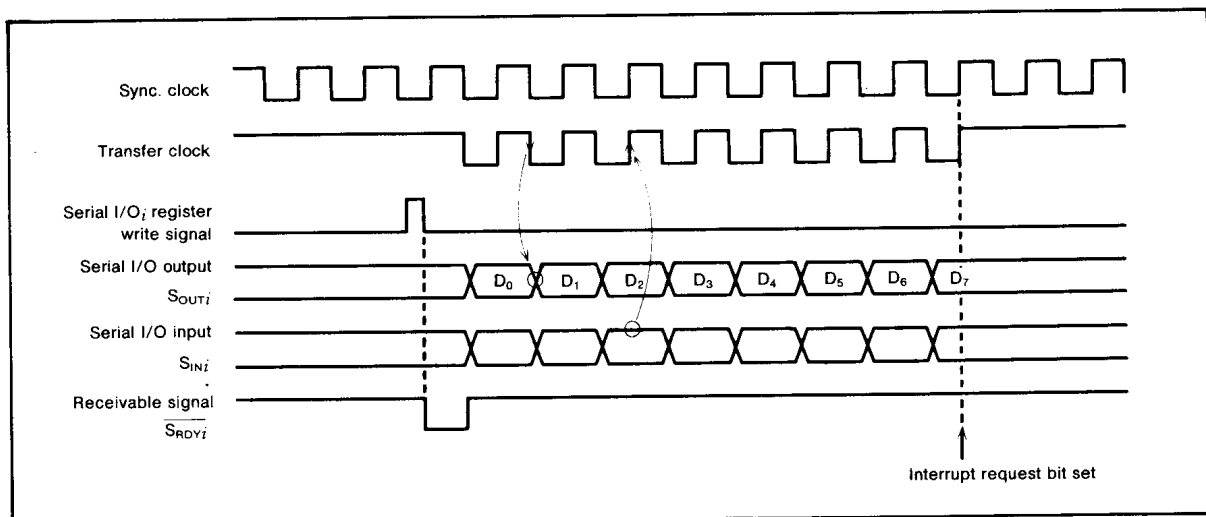


Fig. 8 Serial I/O timing

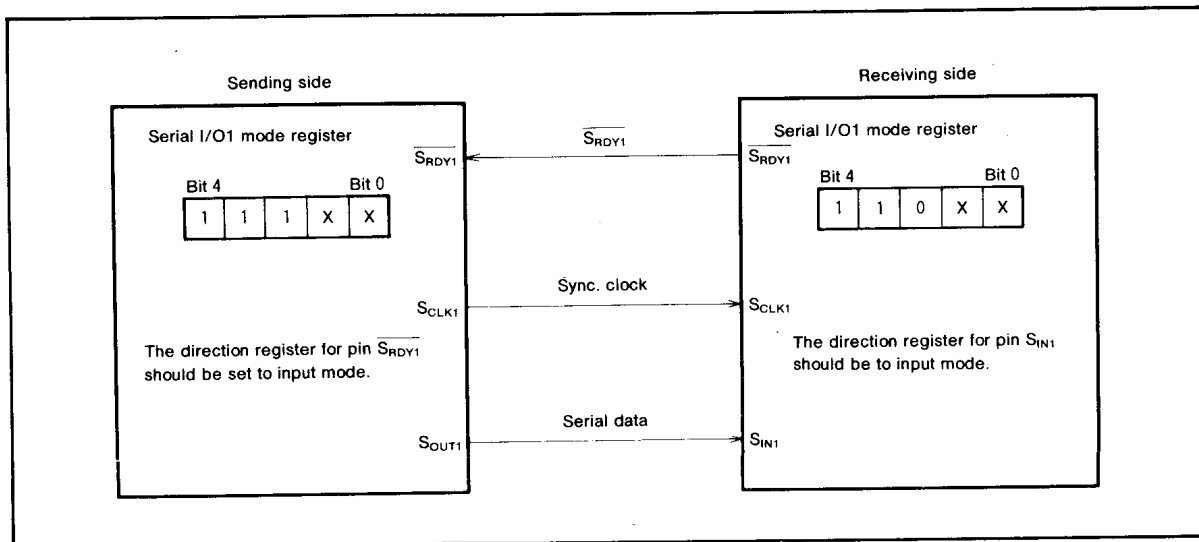


Fig. 9 Example of serial I/O connection

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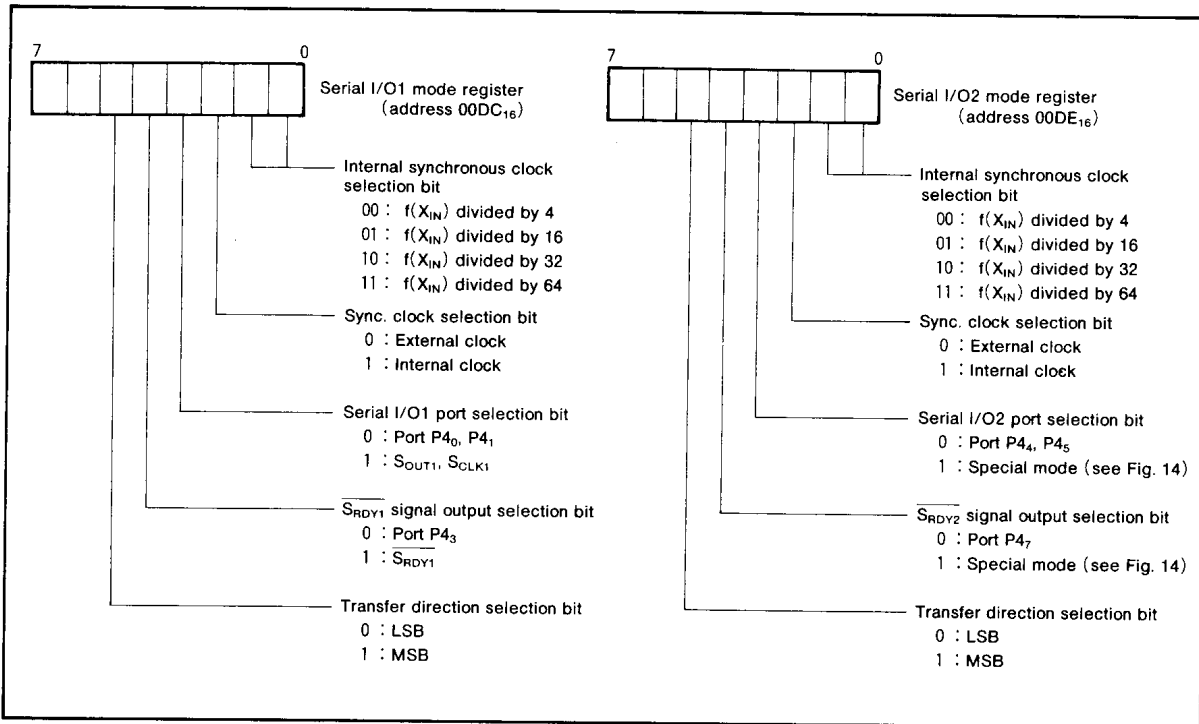


Fig. 10 Structure of serial I/O_i mode register

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SPECIAL MODE (I²C BUS MODE*)

M37102M8-XXXSP has a special serial I/O circuit that can be reception or transmission of serial data in conformity with I²C (Inter IC) bus format.

I²C bus is a two line directional serial bus developed by Philips to transfer and control data among internal IC_S of a machinery.

M37102M8-XXXSP's special serial I/O is not included the clock synchronisation function and the arbitration detectable function at multimaster.

Operations of master transmission and master reception with special serial I/O are explained in the following:

(1) Master transmission

To generate an interrupt at the end of transmission, set bit 7 of special mode register 2 (address 00DB₁₆) to "1" so as to special mode serial I/O interrupt is selected. Then set bit 3 of interrupt control register 2 (address 00FF₁₆) to "1" so as to special mode serial I/O interrupt is enabled. Clear the interrupt disable flag I to "0" by using the CLI instruction.

The output signals of master transmission SDA and SCL are output from ports P₄₄ and P₄₅. Set all bits (bits 4 and 5) corresponding to P₄₄ and P₄₅ of the port P₄ register (address 00C8₁₆) and the port P₄ direction register (address 00C9₁₆) to "1".

Set the transmission clock. The transmission clock uses the overflow signal of timer 4. Set appropriate value in timer 4. (For instance, if f(X_{IN})/16 is selected as the clock source of timer 4 and 4 is set in timer 4 when f(X_{IN}) is 4MHz, the master transmission clock frequency is 25kHz.)

Set contents of the special mode register 2 (address 00DB₁₆). (Usually, "83₁₆".)

Set the bit 3 of serial I/O₂ mode register (address 00DE₁₆). After that set the special mode register 1 (address 00DA₁₆). Figure 14 shows the structure of special mode registers 1 and 2.

Initial setting is completed by the above procedure.

Write data to be transmitted in the special serial I/O regis-

ter (address 00D9₁₆). Immediately after this, clear bits 0 and 1 of special mode register 2 (to "0") to make both SDA and SCL output to "L". This is for arbitration. The start signal has been completed.

The hardware automatically sends out data of 9-clock cycle. The 9th clock is for ACK receiving and the output level becomes "H" at this clock. If other master outputs the start signal to transmit data simultaneously with this 9th clock, it is not detected as an arbitration-lost.

When the ACK bit has been transmitted, bit 3 of the interrupt request register 2 is set to "1" (issue of interrupt request), notifying the end of data transmission.

To transmit data successively, write data to be sent to the special serial I/O register, and set the interrupt enabled state again. By repeating this procedure, unlimited number of bytes can be transmitted.

To terminate data transfer, clear bits 0 and 1 of the special mode register to "0", set bit 1 clock SCL to "1", then set bit 1 data SDA to "1". This procedure transmits the stop signal. Figure 14 shows master transmission timing explained above.

(2) Master reception

Master reception is carried out in the interrupt routine after data is transferred by master transmission. For master transmission and interrupt thereafter, see the preceding section (1) Master transmission.

In the interrupt routine, set master reception ACK provided (26₁₆) in the special mode register 1 (address 00DA₁₆), and write "FF₁₆" in the special serial I/O register (address 00D9₁₆). This sets data line SDA to "H" and to perform 8-clock master reception. Then, "L" is transmitted to data line SDA for ACK receiving. In the ACK provided mode, the above ACK is automatically sent out.

Repeat the above receiving operation for a necessary number of times. Then return to the master transmission mode and transmit the stop signal by the same procedure for the master transmission.

Figure 15 shows master reception timing

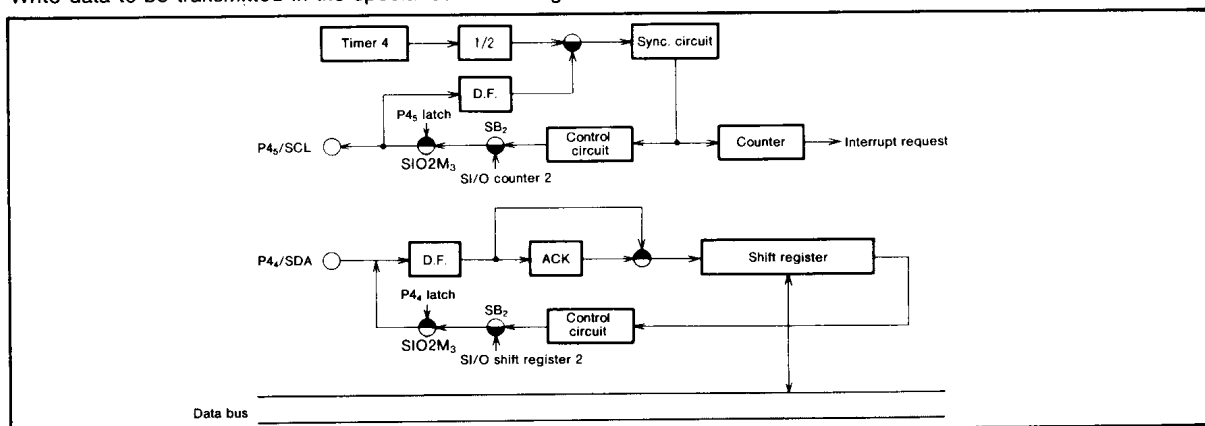


Fig. 11 Block diagram of special serial I/O

* : Purchase of Mitsubishi Electric Corporation's I²C components conveys a license under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

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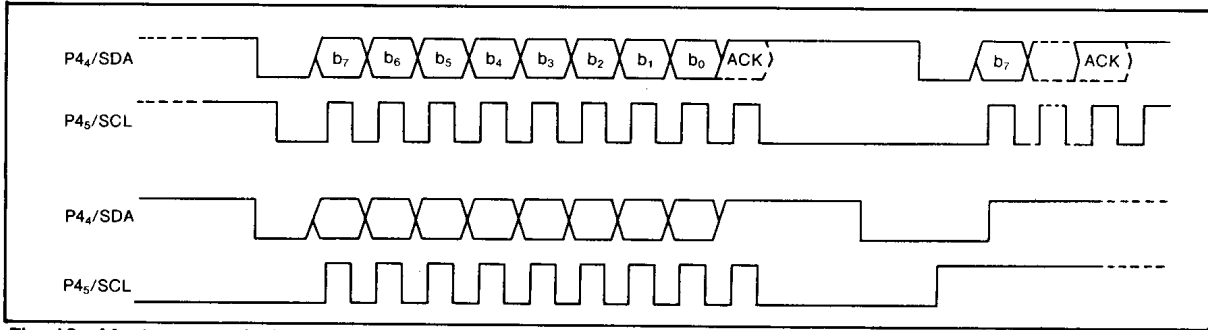


Fig. 12 Master transmission timing

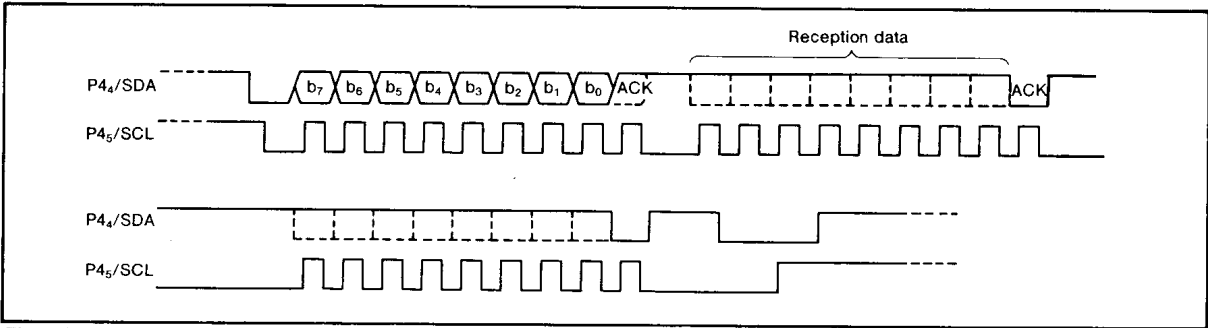


Fig. 13 Master reception timing

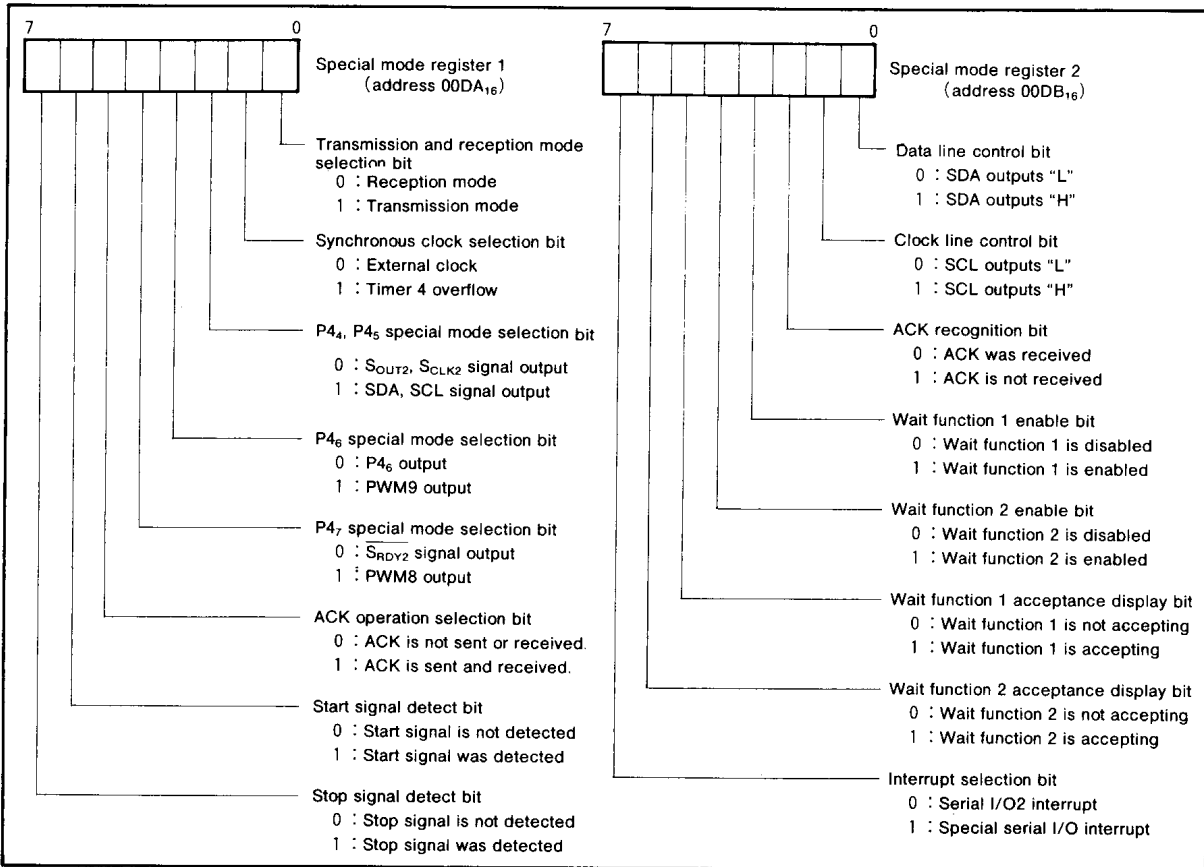


Fig. 14 Structure of special mode registers 1 and 2

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PWM OUTPUT CIRCUIT

(1) Introduction

The M37102M8-XXXSP is equipped with one 14-bit PWM(DA) and ten 8-bit PWMs (PWM0~PWM9). The 14-bit resolution gives DA the minimum resolution bit width of 500ns (for $X_{IN}=4\text{MHz}$) and a repeat period of 8192 μs . PWM0 ~ PWM9 have a 8-bit resolution with minimum resolution bit width of 8 μs and repeat period of 2048 μs .

Block diagram of the PWM is shown in Figure 15.

The PWM timing generator section applies individual control signals to DA and PWM0~9 using clock input X_{IN} divided by 2 as a reference signal.

(2) Data setting

The output pins PWM0~7 are in common with port P6 and PWM8, 9 are in common with port P4₆, P4₇.

For PWM output, each PWM output selection bit (bit 1~7 of PWM output control register 1, bit 0, 1 of PWM output control register 2, bit 3, 4 of special mode register 1 and bit 4 of serial I/O 2 mode register) should be set. When DA is used for output, first set the higher 8-bit of the DA-H register (address 00CE₁₆), then the lower 6-bit of the DA-L register (address 00CF₁₆).

When one of the PWM0~9 is used for output, set the 8-bit in the PWM0 ~ 9 register (address 00D0₁₆ ~ 00D4₁₆, 00F6₁₆~00FA₁₆), respectively.

(3) Transferring data from registers to latches

The data written to the PWM registers is transferred to the PWM latches at the repetition of the PWM period. The signals output to the PWM pins correspond to the contents of these latches. When data in each PWM register is read, data in these latches has already been read allowing the data output by the PWM to be confirmed. However, bit 7 of the DA-L register indicated the completion of the data transfer from the DA register to the DA latch. If bit 7 is "0", the transfer has been completed, if bit 7 is "1", the transfer has not yet begun.

(4) Operation of the 8-bit PWMs

The timing diagram of the ten 8-bit PWMs (PWM0~9) is shown in Figure 16. One period (T) is composed of 256 (2⁸) segments.

There are eight different pulse types configured from bits 0~7 representing the significance of each bit. These are output within one period in the circuit internal section. Refer to Figure 16 (a).

Eight different pulses can be output from the PWM. These can be selected by bits 0 through 7. Depending on the content of the 8-bit PWM latch, pulses from 7~0 is selected. The PWM output is the difference of the sum of each of these pulses. Several examples are shown in Figure 16 (b). Changes in the contents of the PWM latch allows the selection of 256 lengths of high-level area outputs varying from 0/128 to 255/256. An length of entirely high-level output cannot be output, i.e. 256/256.

(5) 14-bit PWM operation

The output example of the 14-bit PWM is shown in Figure 17. The 14-bit PWM divides the data within the PWM latch into the lower 6 bits and higher 8 bits.

A high-level area within a length D_H times τ is output every short area of $t=256 \tau=128\mu\text{s}$ as determined by data D_H of the higher 8 bits.

Thus, the time for the high-level area is equal to the time set by the lower 8 bits or that plus τ . As a result, the short-area period t (= 128 μs , approx. 7.8kHz) becomes an approximately repetitive period.

(6) Output after reset

At reset the output of port P4, P6 is in the high impedance state and the contents of the PWM register and latch are undefined. Note that after setting the PWM register, its data is transferred to the latch.

Table 2. Relation between the 6 lower-order bits of data and high-level area increase space

6 lower-order bits of data	Area longer by τ than that of other t_m ($m = 0 \sim 63$)
0 0 0 0 0 0 ^{LSB}	Nothing
0 0 0 0 0 1	$m=32$
0 0 0 0 1 0	$m=16, 48$
0 0 0 1 0 0	$m=8, 24, 40, 56$
0 0 1 0 0 0	$m=4, 12, 20, 28, 36, 42, 50, 58$
0 1 0 0 0 0	$m=2, 6, 10, 14, 18, 22, 26, 30, 34, 38, 42, 46, 50, 54, 58, 62$
1 0 0 0 0 0	$m=1, 3, 5, 7, \dots, 57, 59, 61, 63$

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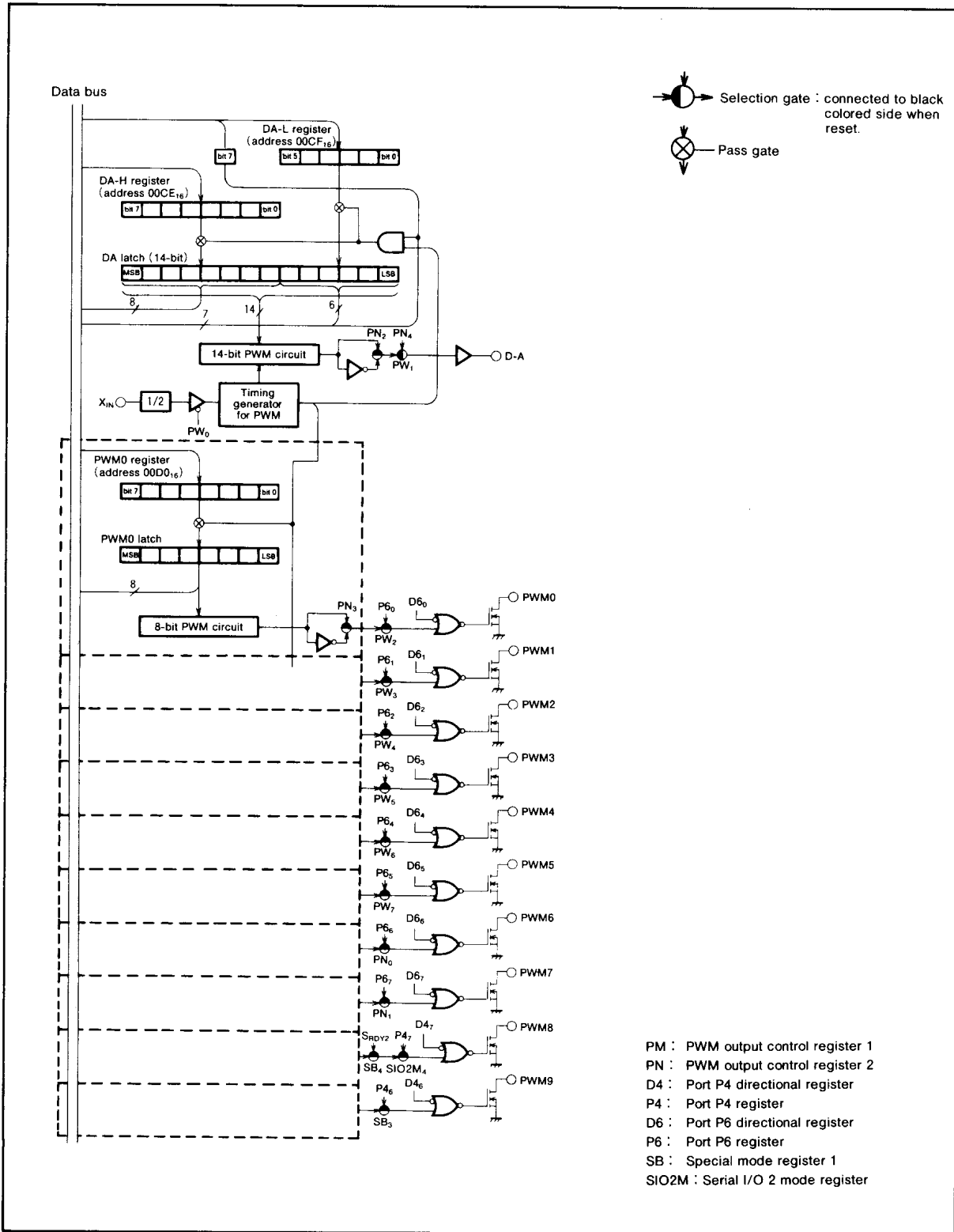


Fig. 15 Block diagram of the PWM circuit

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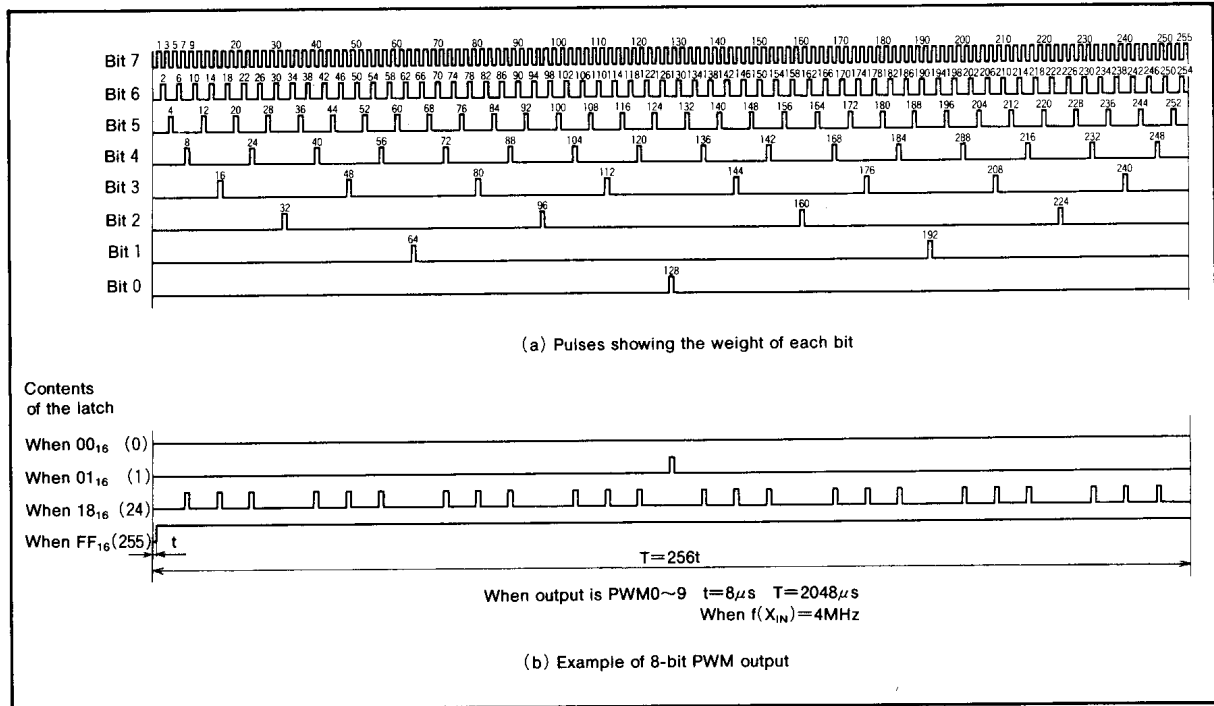


Fig. 16 8-bit PWM timing diagram

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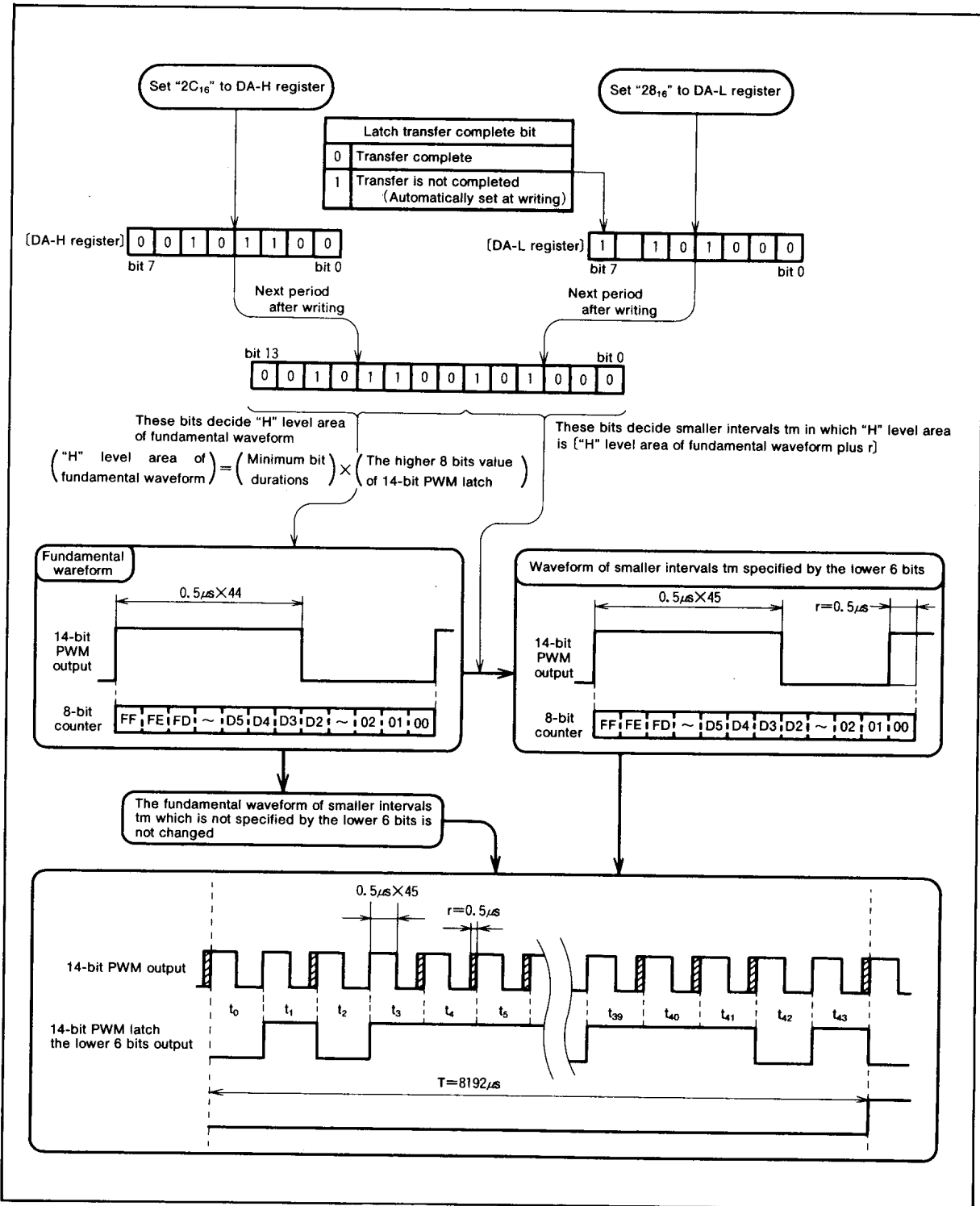


Fig. 17 14-bit PWM output example ($f(X_{1N}) = 4MHz$)

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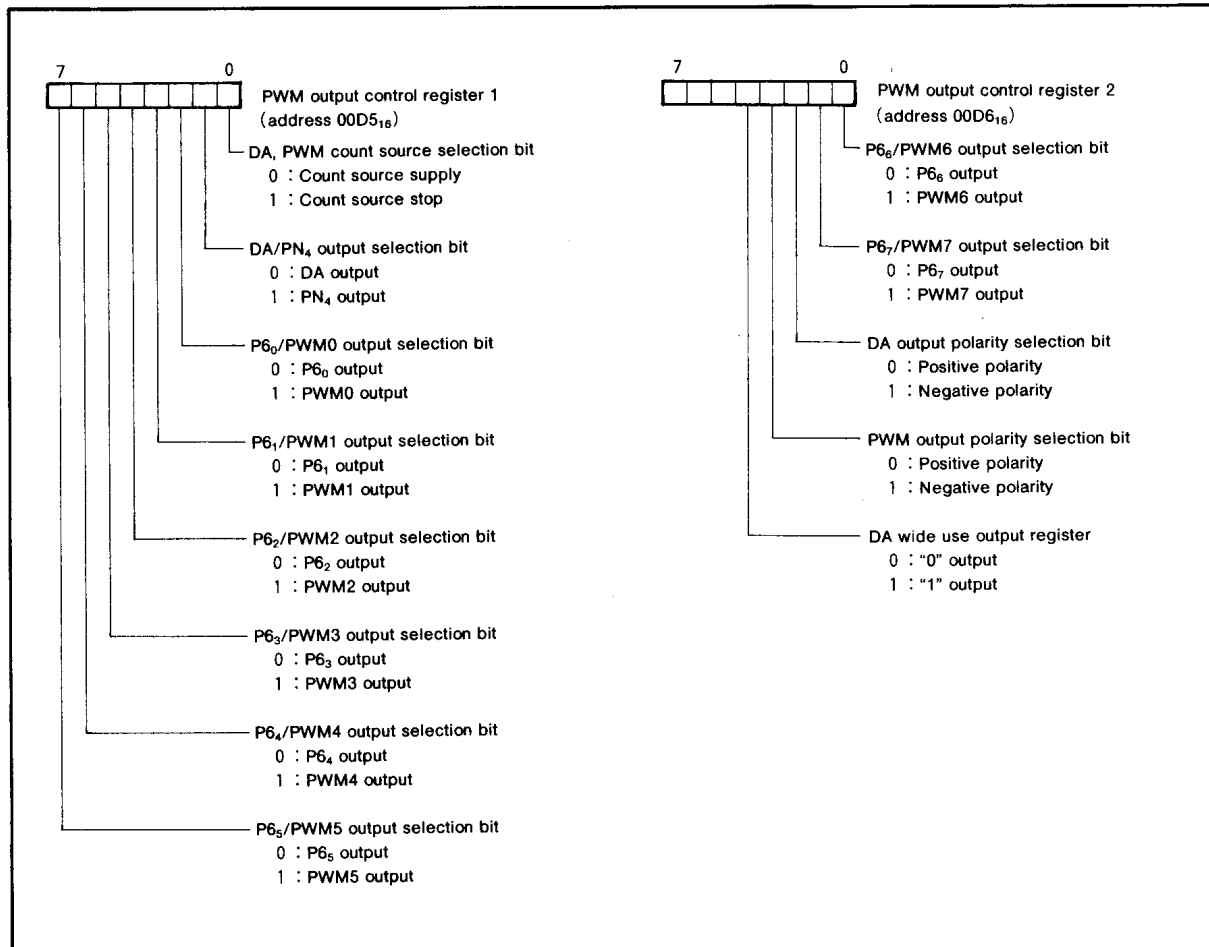


Fig. 18 Structure of PWM output control register 1 and 2

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with ON-SCREEN DISPLAY CONTROLLER**

A-D CONVERTER

Block diagram of A-D converter is shown in Figure 20. A-D converter consists of 4-bit D-A converter and comparator. The A-D control register can generate 1/16 V_{CC} -step internal analog voltage based on the settings of bits 0 to 3.

Table 3 gives the relation between the descriptions of A-D control register bits 0 to 3 and the generated internal analog voltage. The comparison result of the analog input voltage and the internal analog voltage is stored in the A-D control register, bit 4.

The data is compared by setting the directional register corresponding to port $P3_5$, $P3_6$ to "0" (port $P3_5$, $P3_6$ enters the input mode), to allow port $P3_5/A-D1$, $P3_6/A-D2$ to be used as the analog input pin. The digital value corresponding to the internal analog voltage to be compared is then written in the A-D control register, bit 0 to 3 and an analog input pin is selected. After 20 machine cycle, the voltage comparison starts.

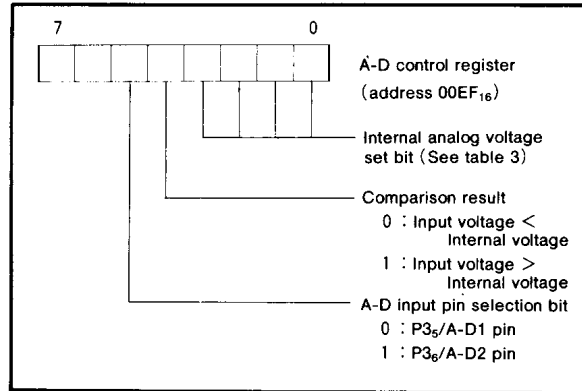


Fig. 19 Structure of A-D control register

Table 3. Relationship between the contents of A-D control register and internal analog voltage

A-D control register				Internal analog voltage
Bit 3	Bit 2	Bit 1	Bit 0	
0	0	0	0	1/32 V_{CC}
0	0	0	1	3/32 V_{CC}
0	0	1	0	5/32 V_{CC}
0	0	1	1	7/32 V_{CC}
0	1	0	0	9/32 V_{CC}
0	1	0	1	11/32 V_{CC}
0	1	1	0	13/32 V_{CC}
0	1	1	1	15/32 V_{CC}
1	0	0	0	17/32 V_{CC}
1	0	0	1	19/32 V_{CC}
1	0	1	0	21/32 V_{CC}
1	0	1	1	23/32 V_{CC}
1	1	0	0	25/32 V_{CC}
1	1	0	1	27/32 V_{CC}
1	1	1	0	29/32 V_{CC}
1	1	1	1	31/32 V_{CC}

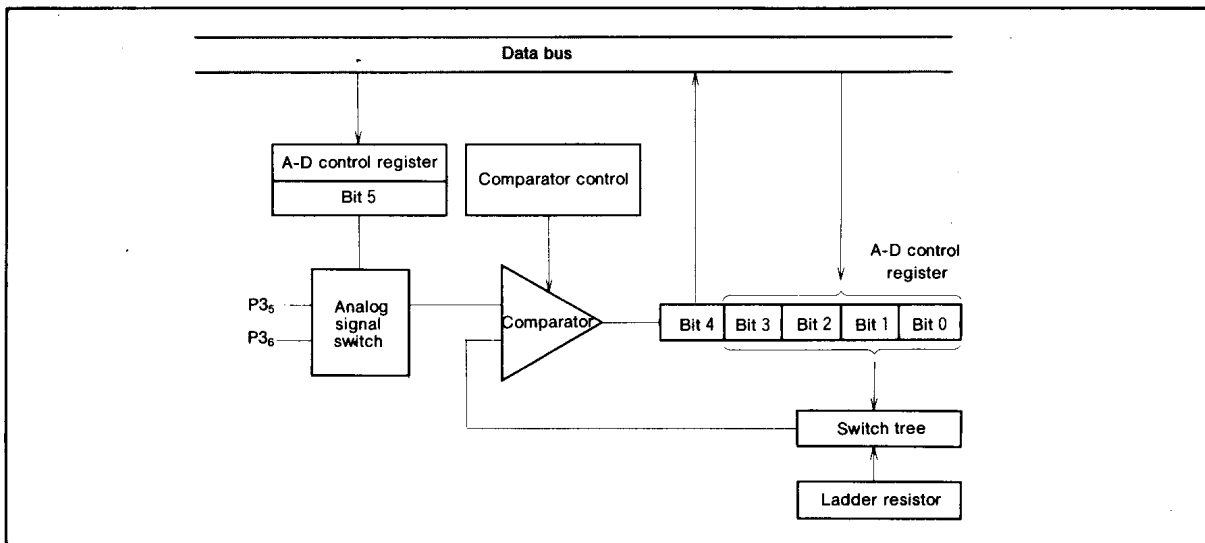


Fig. 20 Block diagram of A-D converter

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CRT DISPLAY FUNCTIONS

(1) Outline of CRT Display Functions

Table 4 outlines the CRT display functions of the M37102M8-XXXSP. The M37102M8-XXXSP incorporates a 24 columns X 3 lines CRT display control circuit. CRT display is controlled by the CRT display control register.

Up to 126 kinds of characters can be displayed, and colors can be specified for each character. Four colors can be displayed on one screen. A combination of up to 15 colors can be obtained by using each output signal (R, G, B, and I).

Characters are displayed in a 12 X 16 dot configuration to obtain smooth character patterns. (See Figure 21)

The following shows the procedure how to display characters on the CRT screen.

Table 4. Outline of CRT display functions

Parameter	Functions	
Number of display character	24 characters X 3 lines	
Character configuration	12 X 16 dots (See Figure 21)	
Kinds of character	126	
Character size	4 size selectable	
Color	Kinds of color	15 (max.)
	Coloring unit	a character
Display expansion	Possible (multiple lines)	

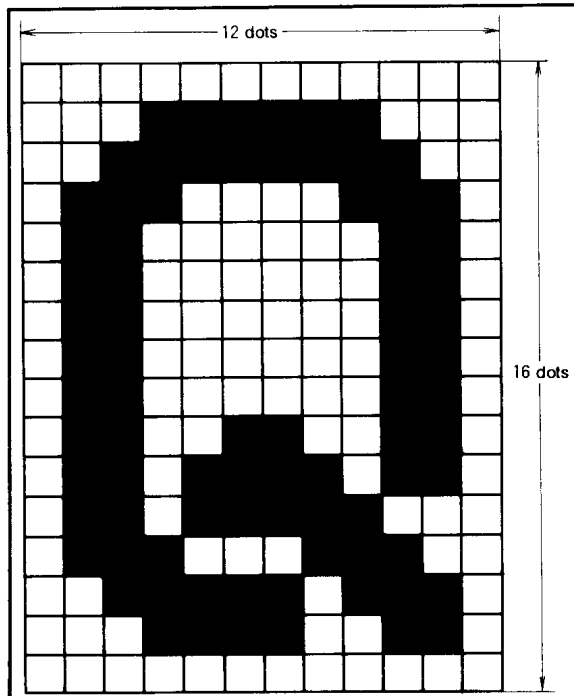


Fig. 21 CRT display character configuration

- ① Set the character to be displayed in display RAM.
- ② Set the display color by using the color register.
- ③ Specify the color register in which the display color is set by using the display RAM.
- ④ Specify the vertical position and character size by using the vertical position register and the character size register.
- ⑤ Specify the horizontal position by using the horizontal position register.
- ⑥ Write the display enable bit to the designated block display flag of the CRT control register. When this is done, the CRT starts operation according to the input of the V_{SYNC} signal.

The CRT display circuit has an extended display mode. This mode allows multiple lines (more than 4 lines) to be displayed on the screen by interrupting the display each time one line is displayed and rewriting data in the block for which display is terminated by software.

Figure 23 shows a block diagram of the CRT display control circuit. Figure 22 shows the structure of the CRT display control register.

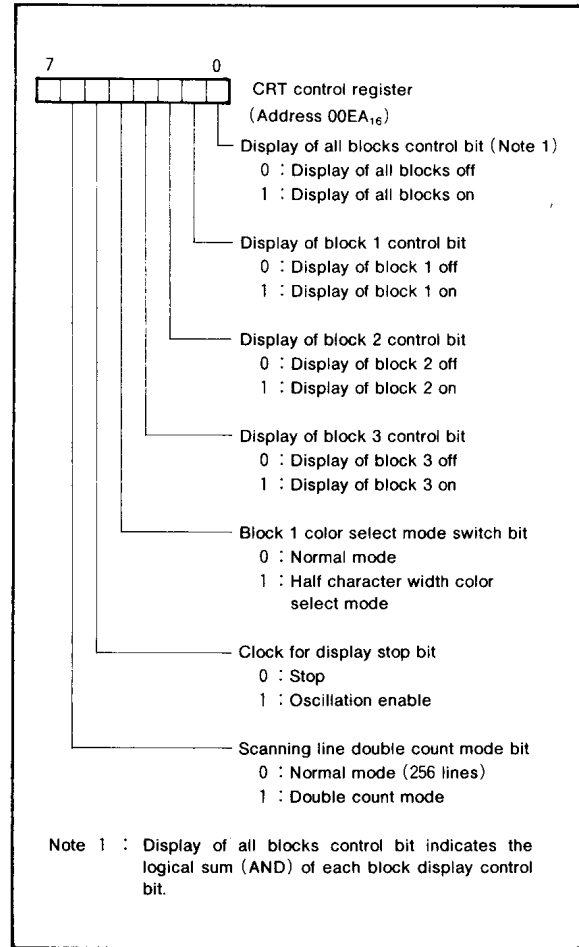


Fig. 22 Structure of CRT control register

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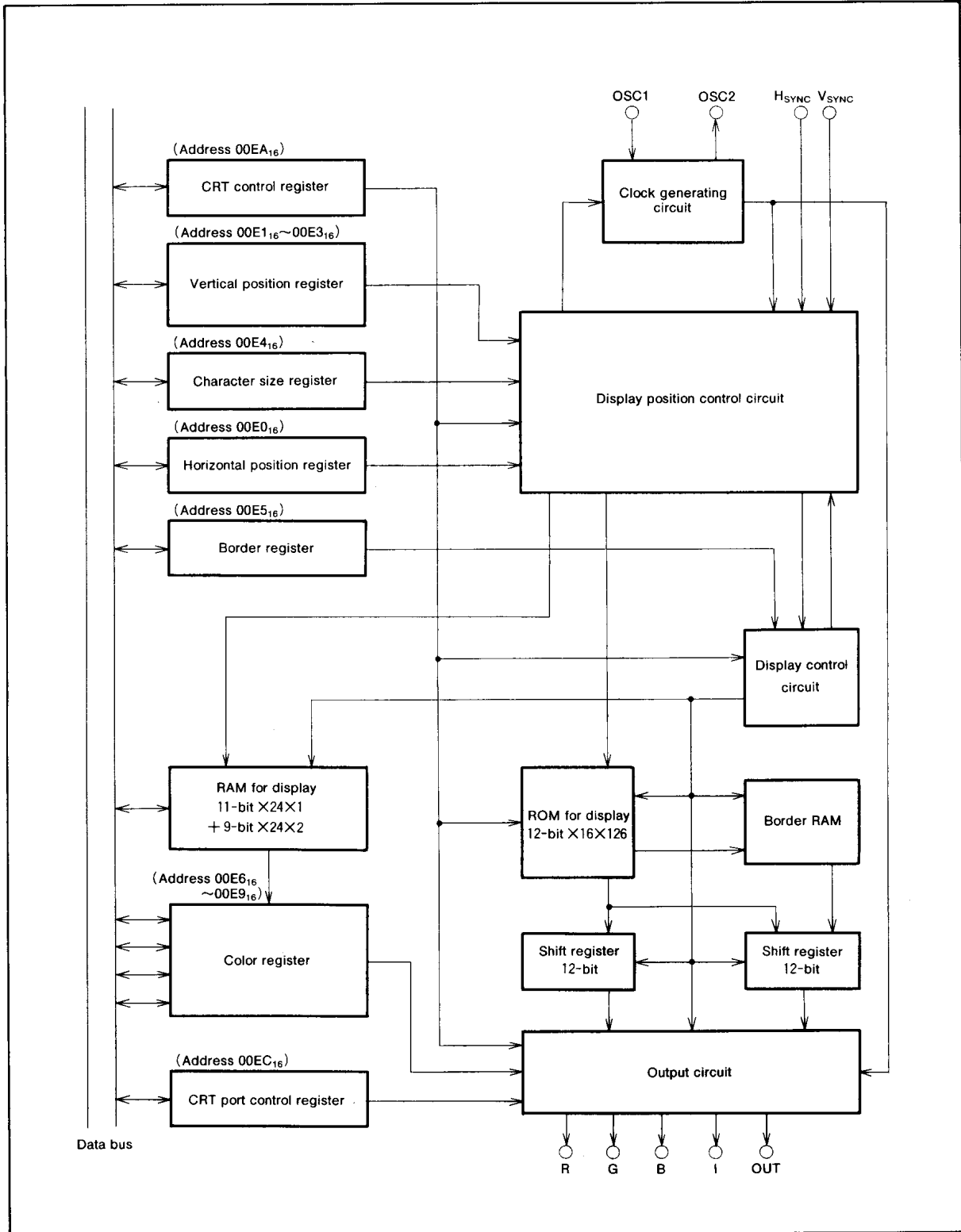


Fig. 23 Block diagram of CRT display control circuit

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(2) Display Position

The display positions of characters are specified in units called a "block." There are three blocks, block 1 to block 3. Up to 24 characters can be displayed in one block. (See (4) Display Memory.)

The display position of each block in both horizontal and vertical directions can be set by software.

The horizontal direction is common to all blocks, and is selected from 64-step display positions in units of $4T_c$ (T_c = oscillation cycle for display).

The display position in the vertical direction is selected from 128-step display positions for each block in units of four scanning lines.

If the display start position of a block overlaps with some other block ((b) in Figure 24), a block of the smaller block No. (1~3) is displayed.

If when one block is displaying, some other block is displayed at the same display position ((c) in Figure 24), the former block is overridden and the latter is displayed.

The vertical position can be specified from 128-step positions (four scanning lines per step) for each block by setting values $00_{16} \sim 7F_{16}$ to bits 0~6 in the vertical position register (addresses $00E1_{16} \sim 00E3_{16}$). Figure 25 shows the structure of the vertical position register.

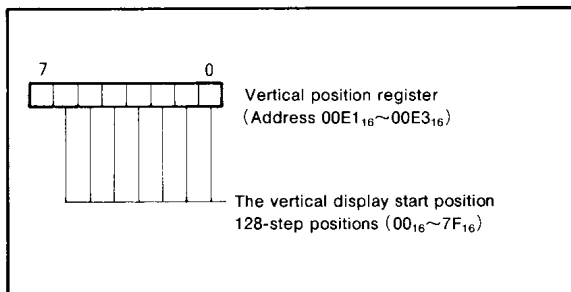


Fig. 24 Structure of vertical position registers

The horizontal direction is common to all blocks, and can be specified from 64-step display positions ($4T_c$ per step (T_c = oscillation cycle for display) by setting values $00_{16} \sim 3F_{16}$ to bits 0~5 in the horizontal position register (address $00E0_{16}$). Figure 26 shows the structure of the horizontal position register.

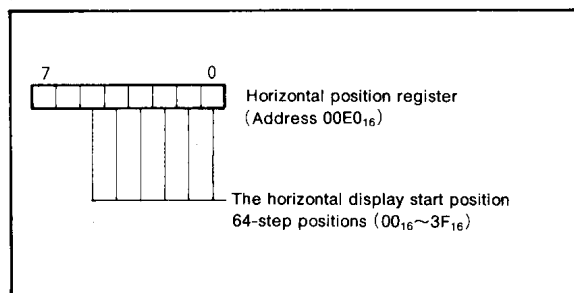


Fig. 25 Structure of horizontal position register

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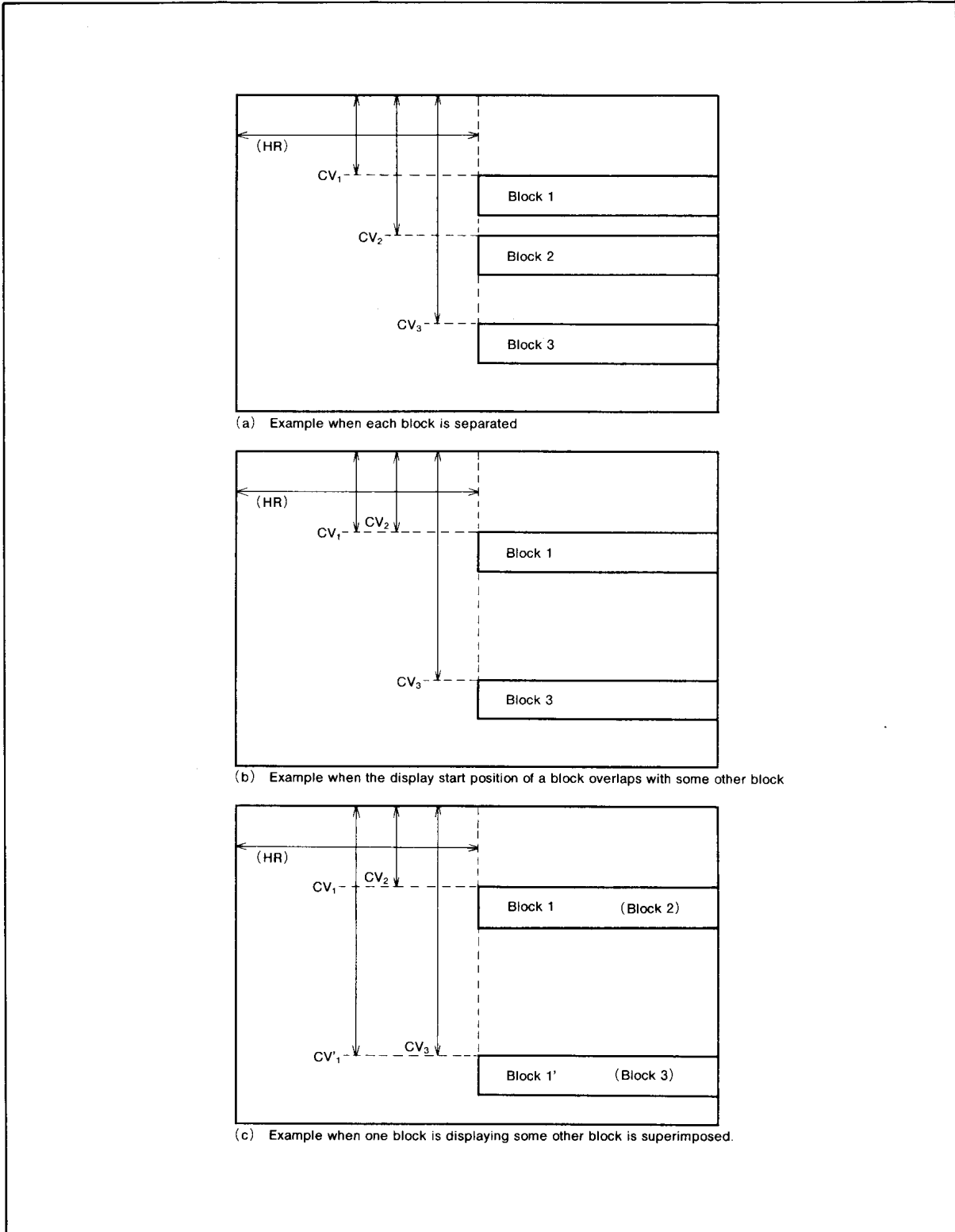


Fig. 26 Display position

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(3) Character Size

The size of characters to be displayed can be selected from four sizes for each block. Use the character size register (address 00E4₁₆) to set a character size. The character size in block 1 can be specified by using bits 0 and 1 in the character size register; the character size in block 2 can be specified by using bits 2 and 3; the character size in block 3 can be specified by using bits 4 and 5. Figure 27 shows the structure of the character size register.

The character size can be selected from four sizes: minimum size, medium size, large size, and extra large size. Each character size is determined by the number of scanning lines in the height (vertical) direction and the cycle of display oscillation ($=T_c$) in the width (horizontal) direction. The minimum size consists of [one scanning line] \times [1 T_c]; the medium size consists of [two scanning lines] \times [2 T_c]; the large size consists of [three scanning lines] \times [3 T_c]; and the extra large size consists of [four scanning lines] \times [4 T_c]. Table 5 shows the relationship between the set values in the character size register and the character sizes.

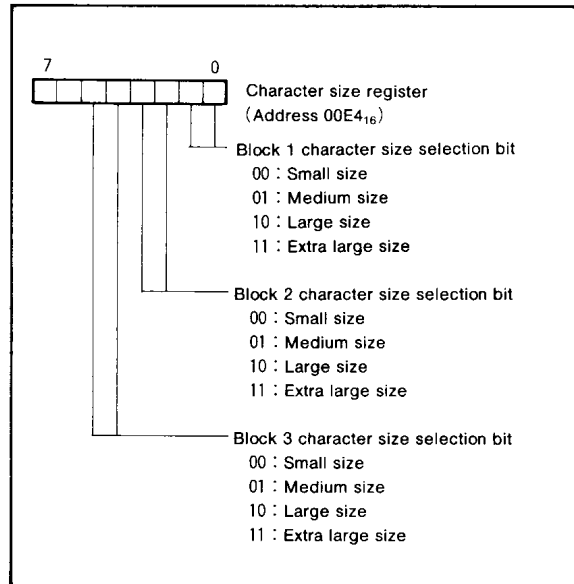


Fig. 27 Structure of character size register

Table 5. The relationship between the set values of the character size register and the character sizes

Set values of the character size register		Character size	Width (horizontal) direction	Height (vertical) direction
CS _{n1}	CS _{n0}			
0	0	Small	1 T_c	1
0	1	Medium	2 T_c	2
1	0	Large	3 T_c	3
1	1	Extra large	4 T_c	4

Note : The display start position in the horizontal direction is not affected by the character size. In other words, the horizontal start position is common to all blocks even when the character size varies with each block. (See Figure 28)

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(4) Display Memory

There are two types of display memory: ROM of CRT display ($3000_{16} \sim 3FFF_{16}$) used to store character dot data (masked) and display RAM ($2000_{16} \sim 20D7_{16}$) used to specify the colors of characters to be displayed. The following describes each type of display memory.

① ROM for CRT display ($3000_{16} \sim 3FFF_{16}$)

The CRT display ROM contains dot pattern data for characters to be displayed. For characters stored in this ROM to be actually displayed, it is necessary to specify them by writing the character code inherent to each character (code determined based on the addresses in the CRT display ROM) into the CRT display RAM.

The CRT display ROM has a capacity of 4K bytes. Because 32 bytes are required for one character data, the ROM can contain up to 128 kinds of characters. Actually, however, because two characters are required for test pattern use, the ROM can contain up to 126 kinds of characters for display use.

The CRT display ROM space is broadly divided into two areas. The [vertical 16 dots] × [horizontal (left side) 8 dots] data of display characters are stored in addresses $3000_{16} \sim 37FF_{16}$; the [vertical 16 dots] × [horizontal (right side) 4 dots] data of display characters are stored in addresses $3800_{16} \sim 3FFF_{16}$. (See Figure 29) Note however that the four upper bits in the data to be written to addresses $3800_{16} \sim 3FFF_{16}$ must be set to "1" (by writing data $F0_{16} \sim FF_{16}$).

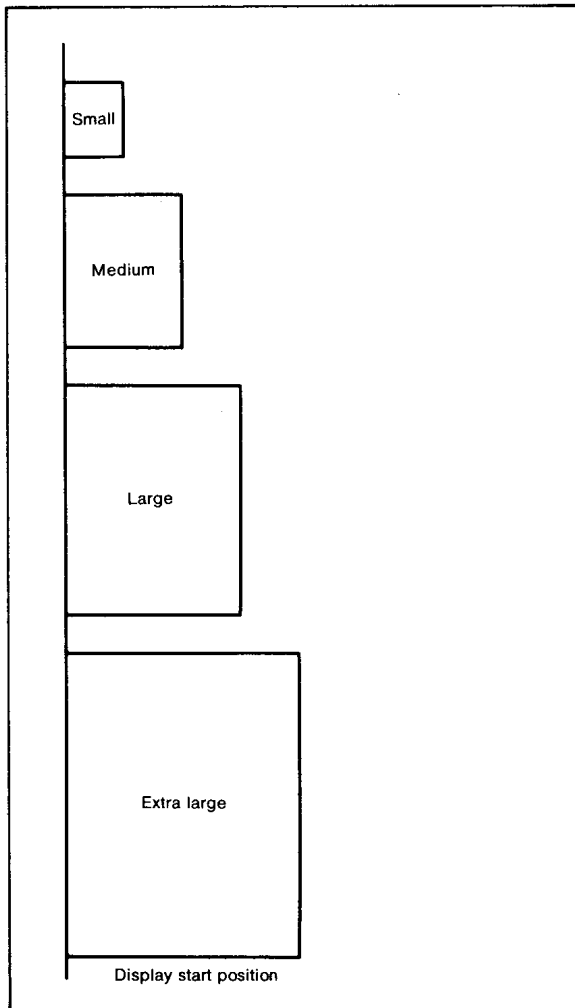


Fig. 28 Display start position of each character size (horizontal direction)

Table 6. Character code list

Character code	Contained up address of character data	
	Left 8 dots lines	Right 4 dots lines
00 ₁₆	3000 ₁₆ } 300F ₁₆	3800 ₁₆ } 380F ₁₆
01 ₁₆	3010 ₁₆ } 301F ₁₆	3810 ₁₆ } 381F ₁₆
02 ₁₆	3020 ₁₆ } 302F ₁₆	3820 ₁₆ } 382F ₁₆
03 ₁₆	3030 ₁₆ } 303F ₁₆	3830 ₁₆ } 383F ₁₆
:	:	:
10 ₁₆	3100 ₁₆ } 310F ₁₆	3900 ₁₆ } 390F ₁₆
11 ₁₆	3110 ₁₆ } 311F ₁₆	3910 ₁₆ } 391F ₁₆
:	:	:
4F ₁₆	34F0 ₁₆ } 34FF ₁₆	3CF0 ₁₆ } 3CFF ₁₆
50 ₁₆	3500 ₁₆ } 350F ₁₆	3D00 ₁₆ } 3D0F ₁₆
:	:	:
7D ₁₆	37D0 ₁₆ } 37DF ₁₆	3FD0 ₁₆ } 3FDF ₁₆
7E ₁₆ *	37E0 ₁₆ } 37EF ₁₆	3FE0 ₁₆ } 3FEF ₁₆
7F ₁₆ *	37F0 ₁₆ } 37FF ₁₆	3FF0 ₁₆ } 3FFF ₁₆

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The character code used to specify a character to be displayed is determined based on the address in the CRT display ROM in which that character is stored.

Assume that data for one character is stored at $3XX0_{16} \sim 3XXF_{16}$ (XX denotes $00_{16} \sim 7F_{16}$) and $3YY0_{16} \sim 3YYF_{16}$ (YY denotes $80_{16} \sim FF_{16}$), then the character code for it is "XX₁₆".

In other words, character code for any given character is configured with two middle digits of the four-digit (hex-notated) address ($3000_{16} \sim 37FF_{16}$) where data for that character is stored.

Table 6 lists the character codes.

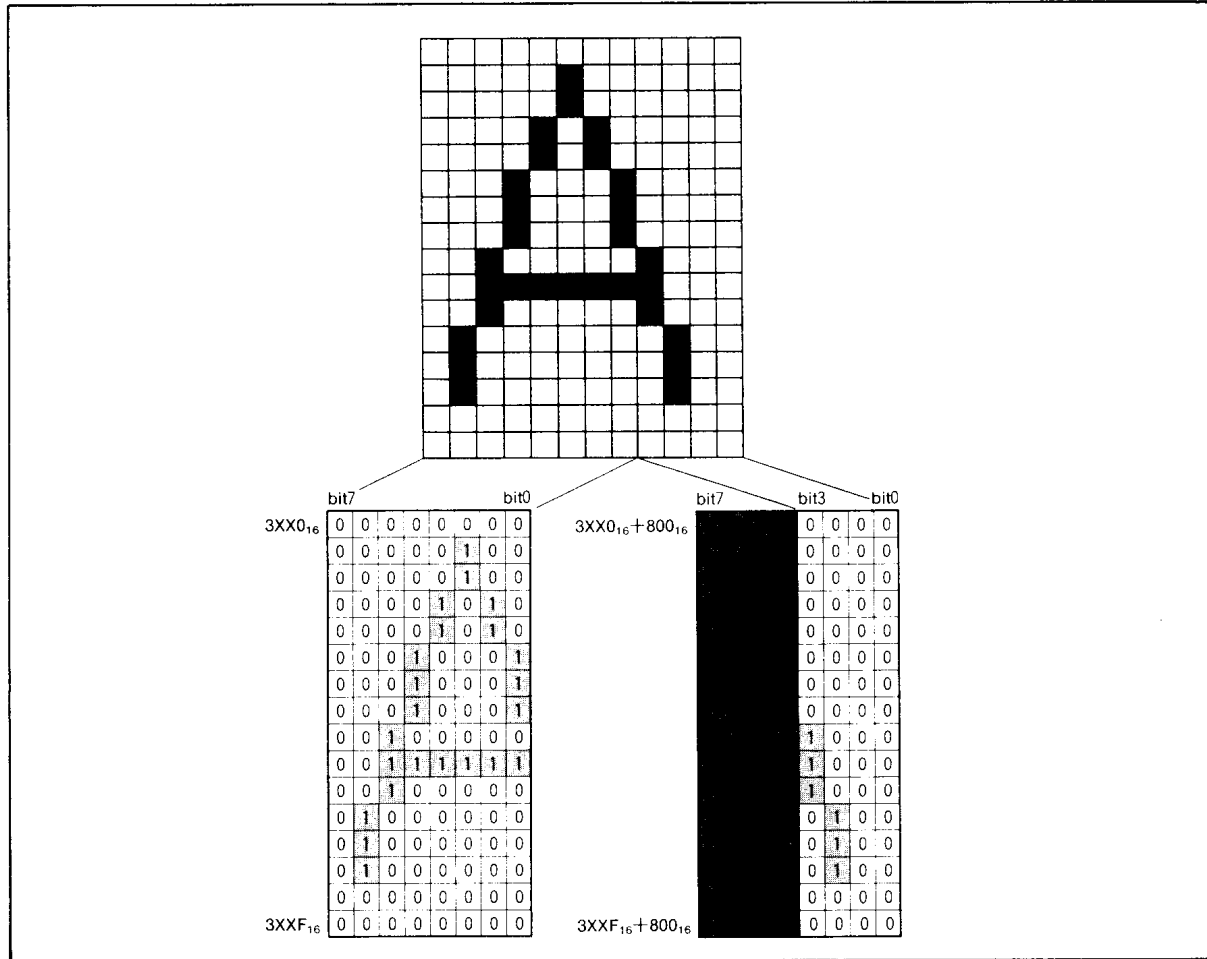


Fig. 29 Display character stored area

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② CRT display RAM (2000₁₆~20D7₁₆)

The CRT display RAM is allocated at addresses 2000₁₆~20D7₁₆, and is divided into a display character code specifying part and display color specifying part for each block. Table 7 shows the contents of the CRT display RAM.

When a character is to be display at the first character (leftmost) position in block 1, for example, it is necessary to write the character code to the seven low-order bits (bits 0~6) in address 2000₁₆ and the color register No. to the two low-order bits (bits 0 and 1) in address 2080₁₆. The color register No. to be written here is one of the four color registers in which the color to be displayed is set in advance. For details on color registers, refer to (6) Color Registers.

The structure of the CRT display RAM is shown in Figure 30. Write the character patterns at Table 8 and 9, when M37102M8-XXXSP is mask-ordered.

Table 7. The contents of the CRT display RAM

Block	Display position (from left)	Character code specification	Color specification
Block 1	1st column	2000 ₁₆	2080 ₁₆
	2nd column	2001 ₁₆	2081 ₁₆
	3rd column	2002 ₁₆	2082 ₁₆
	⋮	⋮	⋮
	22th column	2015 ₁₆	2095 ₁₆
	23th column	2016 ₁₆	2096 ₁₆
	24th column	2017 ₁₆	2097 ₁₆
Not used		2018 ₁₆	2098 ₁₆
		}	}
		201F ₁₆	209F ₁₆
Block 2	1st column	2020 ₁₆	20A0 ₁₆
	2nd column	2021 ₁₆	20A1 ₁₆
	3rd column	2022 ₁₆	20A2 ₁₆
	⋮	⋮	⋮
	22th column	2035 ₁₆	20B5 ₁₆
	23th column	2036 ₁₆	20B6 ₁₆
	24th column	2037 ₁₆	20B7 ₁₆
Not used		2038 ₁₆	20B8 ₁₆
		}	}
		203F ₁₆	20BF ₁₆
Block 3	1st column	2040 ₁₆	20C0 ₁₆
	2nd column	2041 ₁₆	20C1 ₁₆
	3rd column	2042 ₁₆	20C2 ₁₆
	⋮	⋮	⋮
	22th column	2055 ₁₆	20D5 ₁₆
	23th column	2056 ₁₆	20D6 ₁₆
	24th column	2057 ₁₆	20D7 ₁₆
Not used		2058 ₁₆	
		}	
		207F ₁₆	

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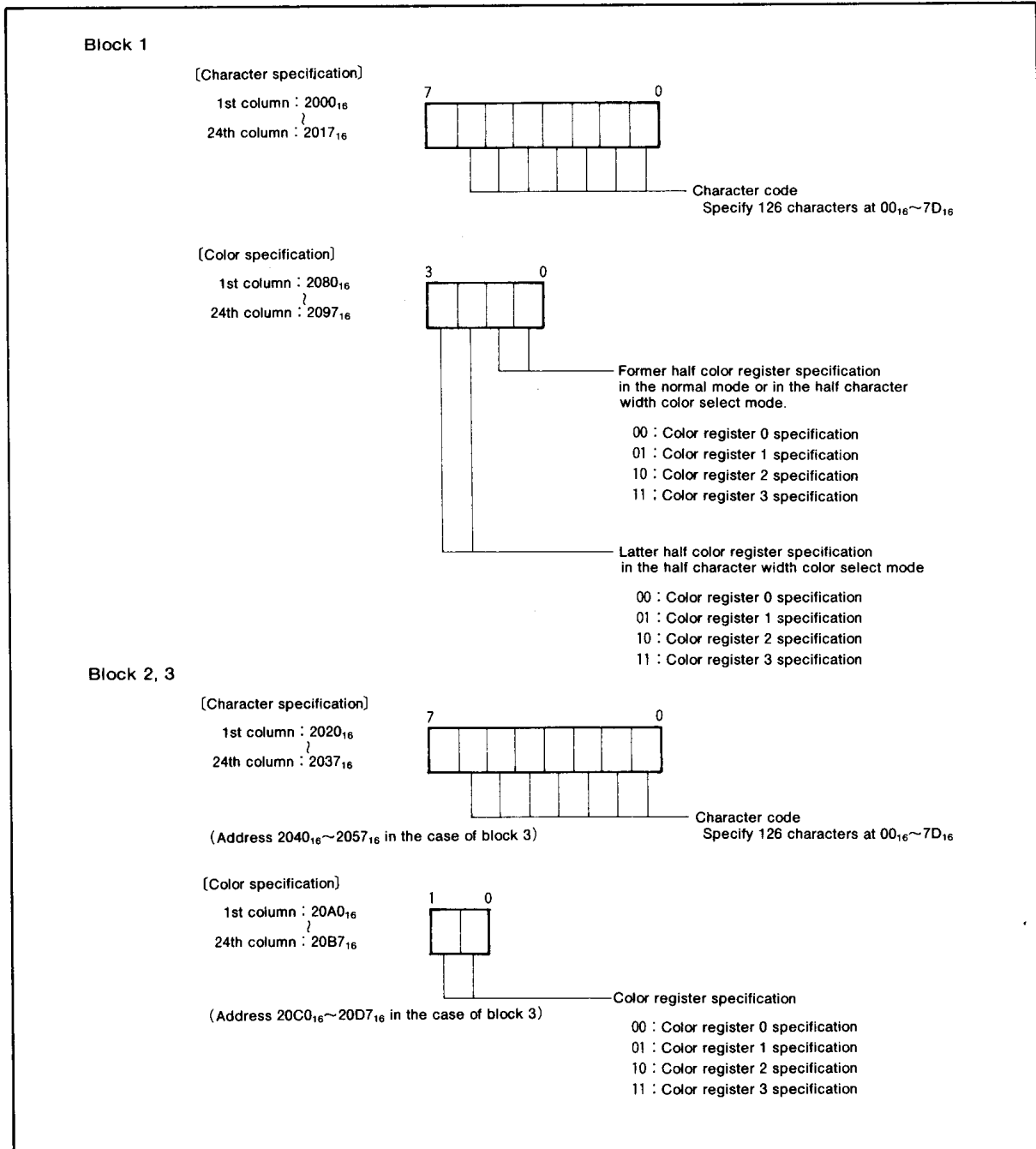


Fig. 30 Structure of the CRT display RAM

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Table 8. Test character patterns 1

Address	Data	Address	Data
37E0 ₁₆	40 ₁₆	3FE0 ₁₆	F0 ₁₆
37E1 ₁₆	04 ₁₆	3FE1 ₁₆	F0 ₁₆
37E2 ₁₆	00 ₁₆	3FE2 ₁₆	F4 ₁₆
37E3 ₁₆	20 ₁₆	3FE3 ₁₆	F0 ₁₆
37E4 ₁₆	02 ₁₆	3FE4 ₁₆	F0 ₁₆
37E5 ₁₆	00 ₁₆	3FE5 ₁₆	F2 ₁₆
37E6 ₁₆	10 ₁₆	3FE6 ₁₆	F0 ₁₆
37E7 ₁₆	01 ₁₆	3FE7 ₁₆	F0 ₁₆
37E8 ₁₆	80 ₁₆	3FE8 ₁₆	F0 ₁₆
37E9 ₁₆	08 ₁₆	3FE9 ₁₆	F0 ₁₆
37EA ₁₆	00 ₁₆	3FEA ₁₆	F8 ₁₆
37EB ₁₆	40 ₁₆	3FEB ₁₆	F0 ₁₆
37EC ₁₆	04 ₁₆	3FEC ₁₆	F0 ₁₆
37ED ₁₆	00 ₁₆	3FED ₁₆	F4 ₁₆
37EE ₁₆	20 ₁₆	3FEE ₁₆	F0 ₁₆
37EF ₁₆	02 ₁₆	3FEF ₁₆	F0 ₁₆

Table 9. Test character patterns 2

Address	Data	Address	Data
37F0 ₁₆	00 ₁₆	3FF0 ₁₆	F0 ₁₆
37F1 ₁₆	00 ₁₆	3FF1 ₁₆	F0 ₁₆
37F2 ₁₆	00 ₁₆	3FF2 ₁₆	F0 ₁₆
37F3 ₁₆	00 ₁₆	3FF3 ₁₆	F0 ₁₆
37F4 ₁₆	00 ₁₆	3FF4 ₁₆	F0 ₁₆
37F5 ₁₆	00 ₁₆	3FF5 ₁₆	F0 ₁₆
37F6 ₁₆	00 ₁₆	3FF6 ₁₆	F0 ₁₆
37F7 ₁₆	00 ₁₆	3FF7 ₁₆	F0 ₁₆
37F8 ₁₆	00 ₁₆	3FF8 ₁₆	F0 ₁₆
37F9 ₁₆	00 ₁₆	3FF9 ₁₆	F0 ₁₆
37FA ₁₆	00 ₁₆	3FFA ₁₆	F0 ₁₆
37FB ₁₆	00 ₁₆	3FFB ₁₆	F0 ₁₆
37FC ₁₆	00 ₁₆	3FFC ₁₆	F0 ₁₆
37FD ₁₆	00 ₁₆	3FFD ₁₆	F0 ₁₆
37FE ₁₆	00 ₁₆	3FFE ₁₆	F0 ₁₆
37FF ₁₆	00 ₁₆	3FFF ₁₆	F0 ₁₆

(5) Color Registers

The color of a displayed character can be specified by setting the color to one of the four color registers (CO0~CO3: addresses 00E6₁₆~00E9₁₆) and then specifying that color register with the CRT display RAM.

There are four color outputs: R, G, B, and I. By using a combination of these outputs, it is possible to set 2^4-1 (when no output) = 15 colors. However, because only four color registers are available, up to four colors can be displayed at one time.

R, G, B, and I outputs are set by using bits 0~3 in the color register. Bit 4 in the color register is used to set a character or blank output; bit 5 is used to specify whether a character output or blank output. Figure 31 shows the structure of the color register.

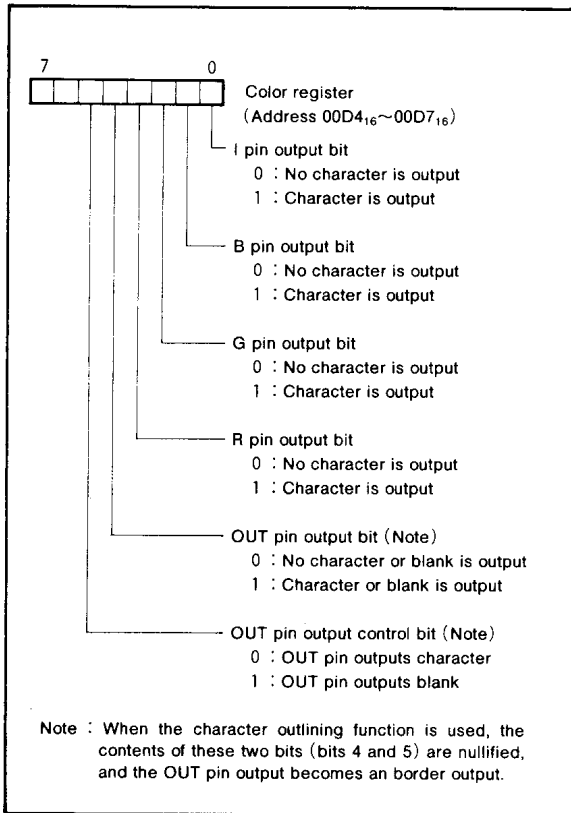


Fig. 31 Structure of color registers

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(6) Half Character Width Color Select Mode

By setting "1" to bit 4 in the CRT control register (address $00EA_{16}$) it is possible to specify colors in units of a half character size (vertical 16 dots×horizontal 6 dots) for characters in block 1 only.

In the half character width color select mode, colors of display characters in block 1 are specified as follows:

- ① The left half of the character is set to the color of the color register that is specified by bits 0 and 1 at the color register specifying addresses in the CRT display RAM (addresses $2080_{16} \sim 2097_{16}$).
- ② The right half of the character is set to the color of the color register that is specified by bits 2 and 3 at the color register specifying address in the CRT display RAM (addresses $2080_{16} \sim 2097_{16}$).

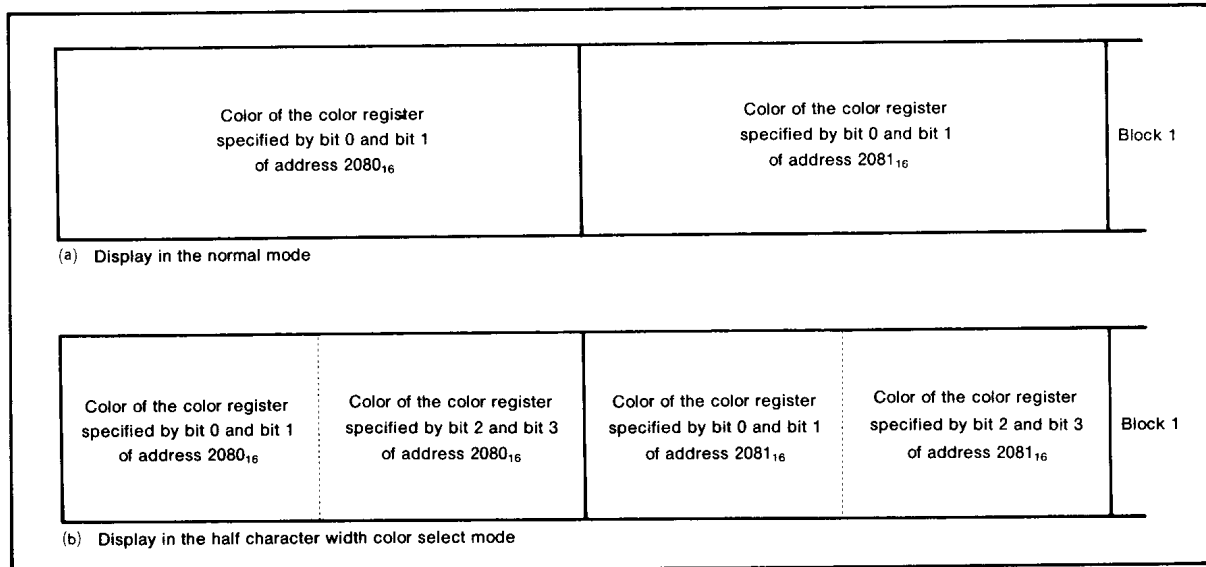


Fig. 32 Difference between normal color select mode and half character width color select mode

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(7) Multiline Display

The M37102M8-XXXSP can normally display three lines on the CRT screen by displaying three blocks at different horizontal positions.

In addition, it allows up to 16 lines to be displayed by using a CRT interrupt and display block counter.

The CRT interrupt works in such a way that when display of one block is terminated, an interrupt request is generated. In other words, character display for a certain block is initiated when the scanning line reaches the display position for that block (specified with vertical and horizontal position registers) and when the range of that block is exceeded, an interrupt is applied.

The display block counter is used to count the number of blocks that have just been displayed. Each time the display of one block is terminated, the contents of the counter are incremented by one.

For multiline display, it is necessary to enable the CRT interrupt (by clearing the interrupt disable flag to "0" and setting the CRT interrupt enable bit=bit 4 at address 00FE₁₆) to "1", then execute the following processing in the CRT interrupt handling routine.

- ① Read the value of the display block counter.
- ② The block for which display is terminated (i.e., the cause of CRT interrupt generation) can be determined by the value read in ①.
- ③ Replace the display character data and display position of that block with the character data (contents of CRT display RAM) and display position (contents of vertical position and horizontal position registers) to be displayed next.

Figure 33 shows the structure of the display block counter.

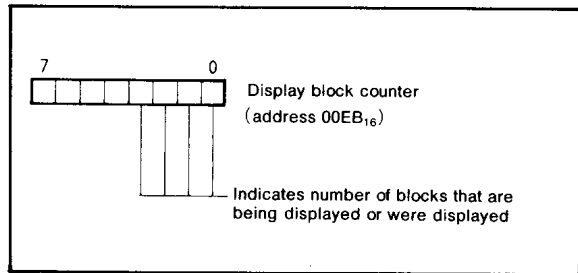


Fig. 33 Structure of display block counter

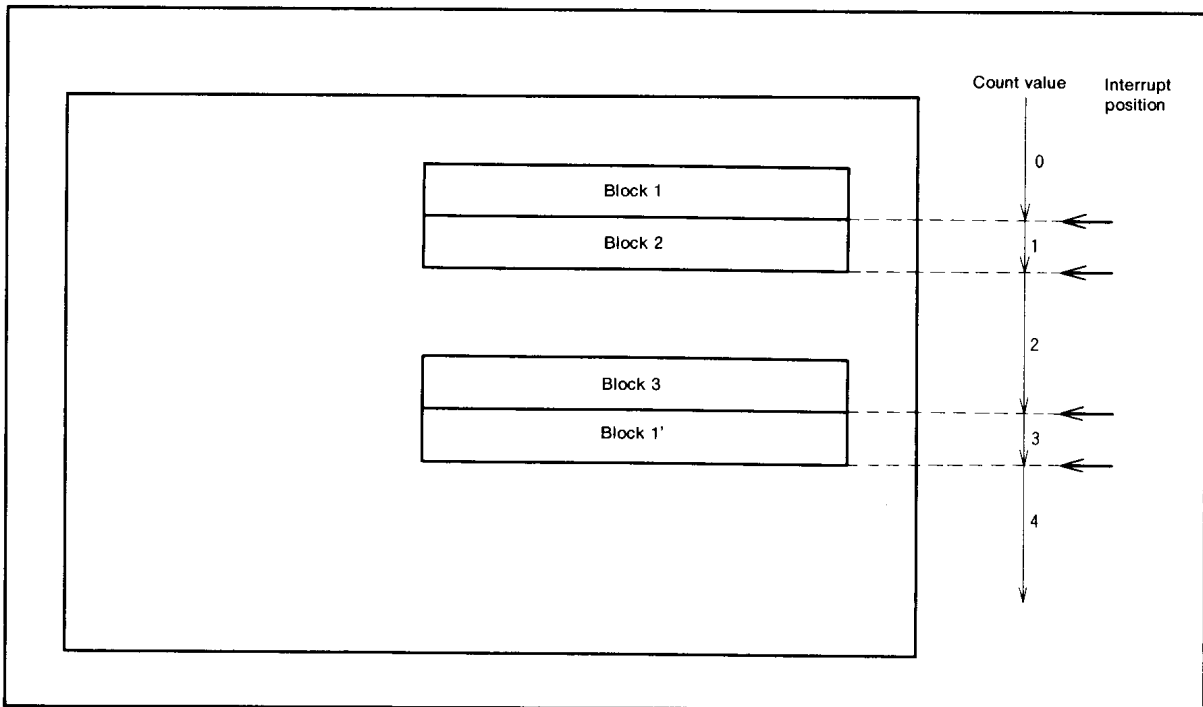


Fig. 34 Timing of CRT interrupt and count value of display block counter

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(8) Scanning Line Double Count Mode

One dot in a displayed character is normally shown by one scanning line. In the scanning line double count mode, one dot can be shown by two scanning lines. As a result, the displayed dot is extended two times the normal size in the vertical direction only. (That is to say, the height of a character is extended twofold.)

In addition, because the scanning line count is doubled, the display start position of a character is also extended twofold in the vertical direction. In other words, whereas the contents set in the vertical position register in the normal mode are 128 steps from 00_{16} to $7F_{16}$, or four scanning lines per step, the number of steps in the scanning line double count mode is 64 from 00_{16} to $3F_{16}$, or eight scanning lines per step.

If the contents of the vertical position register for a block are set in the address range of 40_{16} to $7F_{16}$ in the scanning line double count mode, that block cannot be displayed (not output to the CRT screen).

In the scanning line double count mode can be specified by setting bit 6 in the CRT control register (address $00EA_{16}$) to "1".

Because this function works in units of screen, even when the mode is changed the mode about the scanning line count during display of one screen, the double count mode only becomes valid from the time the next screen is displayed.

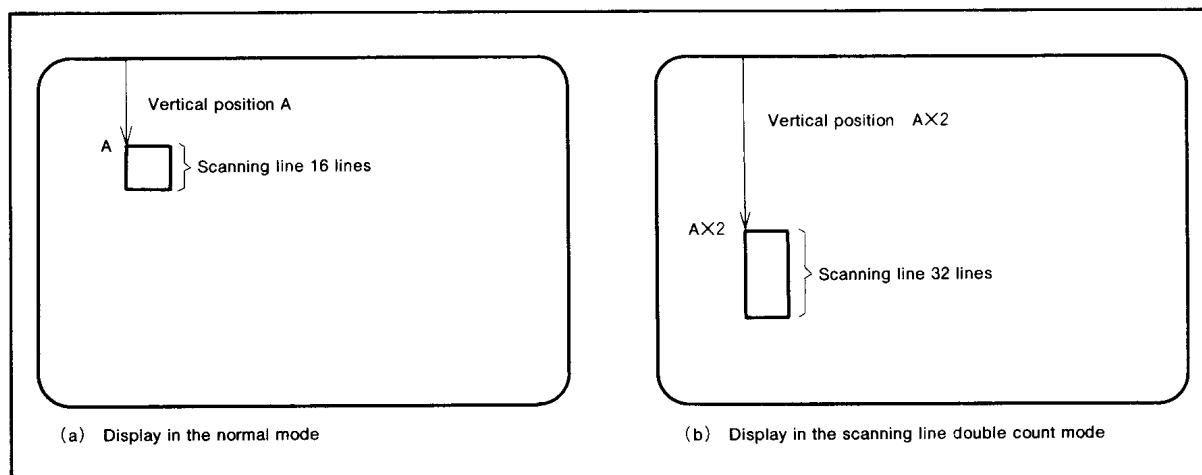


Fig. 35 Display in the normal mode and in the scanning line double count mode

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(9) Character Border Function

An border of a one clock (one dot) equivalent size can be added to a character to be displayed in both horizontal and vertical directions.

The border is output from the OUT pin. In this case, bits 4 and 5 in the color register (contents output from the OUT pin) are nullified, and the border is output from the OUT pin instead.

Border can be specified in units of block by using the border select register (address 00E5₁₆). Table 10 shows the relationship between the values set in the border select register and the character border function. Figure 37 shows the structure of the border select register.

Table 10. The relationship between the value set in the border selection register and the character border function

Border selection register		Functions	Example of output
MDn1	MDn0		
X	0	Normal	R, G, B, I output OUT output
0	1	Border including character	R, G, B, I output OUT output
1	1	Border not including character	R, G, B, I output OUT output

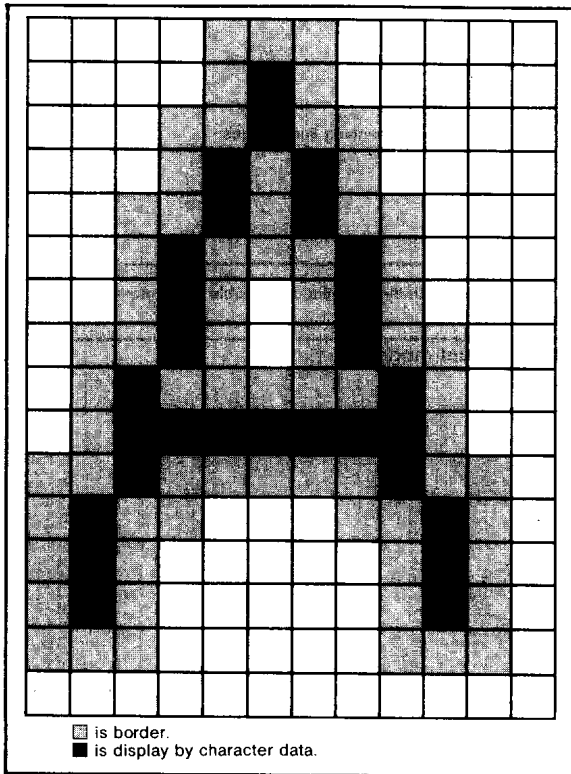


Fig. 36 Example of border

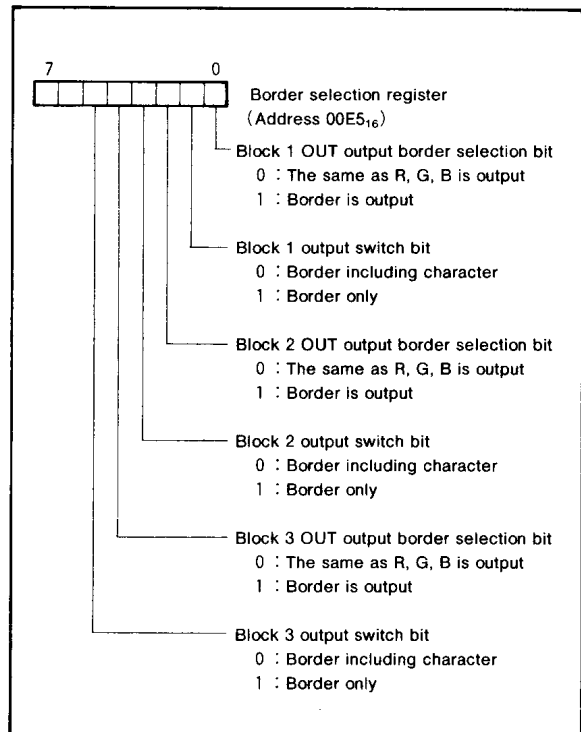


Fig. 37 Structure of border selection register

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(10) CRT Output Pin Control

CRT output pins R, G, B, I, and OUT are respectively shared with port P5₂, P5₃, P5₄, P5₅, and P5₆. When the corresponding bits in the port P5 direction register are cleared to "0", the pins are set for CRT output; when the bits are set to "1", the pins function as port P5 (general-purpose output pins).

The polarities of CRT outputs (R, G, B, I, and OUT, as well as H_{SYNC} and V_{SYNC}) can be specified by using the CRT port control register (address 00EC₁₆).

Use bits 0~4 in the CRT port control register to set the output polarities of H_{SYNC}, V_{SYNC}, R/G/B, I, and OUT. When these bits are cleared to "0", a positive polarity is selected; when the bits are set to "1", a negative polarity is selected. Bits 5~7 in the CRT port control register are used to specify pin by pin whether normal video signals or R-MUTE, G-MUTE, and B-MUTE signals are output from each pin (R, G, B). When set for R-MUTE, G-MUTE, and B-MUTE outputs, the whole background colors of the screen become red, green, and blue.

Figure 38 shows the structure of the CRT port control register.

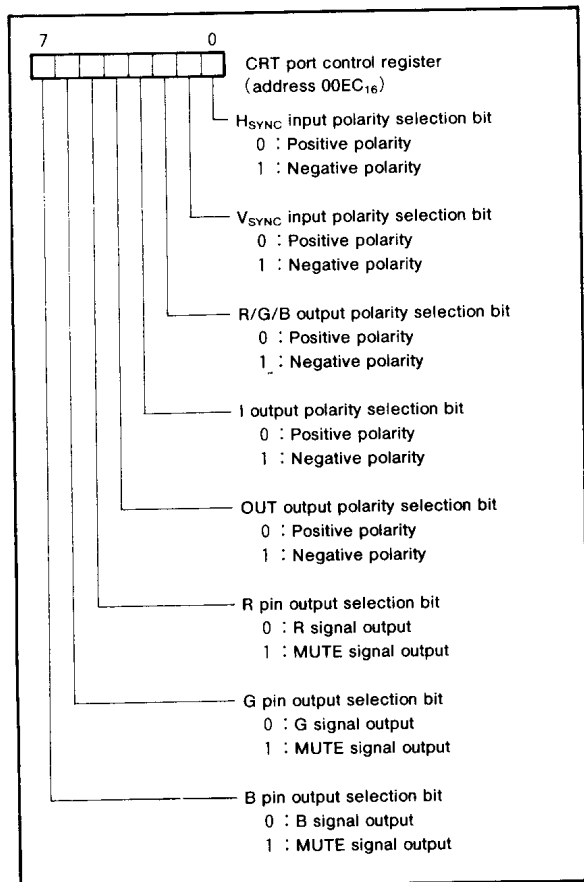


Fig. 38 Structure of CRT port control register

(11) Scroll Function

① Scroll mode

The M37102M8-XXXSP allows the display area to be gradually expanded or shrunk in the vertically direction in units of 1H (H: H_{SYNC} signal). There are three modes for this scroll method. Each mode has Down and UP modes, providing a total of six modes.

Table 11 shows the contents of each scroll mode.

② Scroll speed

The scroll speed is determined by the vertical synchronization (V_{SYNC}) signal. For the NTSC interlace method, assuming that

$$V = 16.7\text{ms} \quad 262.5 \text{ H}_{\text{SYNC}} \text{ signals per screen}$$

we obtain the scroll speed as shown in Table 12.

Scroll resolution varies with each scroll mode. In mode 1 and mode 2, one of three resolutions (1H, 2H, 4H) can be selected. In mode 3, scroll is done in units of 4H alone.

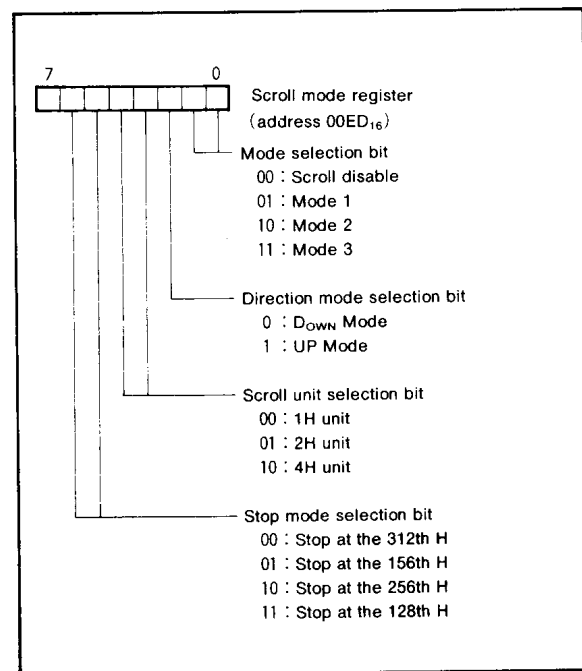


Fig. 39 Structure of scroll mode register

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Table 11. Scroll operation in each mode and the values of scroll mode register

Mode		Scroll operation	Scroll mode register			
			Bit 2	Bit 1	Bit 0	
1	DOWN	Appear from upper side		0	0	1
	UP	Erase from lower side		1	0	1
2	DOWN	Erase from upper side		0	1	0
	UP	Appear from lower side		1	1	0
3	DOWN	Erase from both upper and lower side		0	1	1
	UP	Appear to both upper and lower side		1	1	1

Table 12. Scroll speed

Scroll resolution	Scroll speed (in all picture)
1 H unit	$16.7 \text{ (ms)} \times 262.5 \div 1 \approx 4 \text{ (s)}$
2 H unit	$16.7 \text{ (ms)} \times 262.5 \div 2 \approx 2 \text{ (s)}$
4 H unit	$16.7 \text{ (ms)} \times 262.5 \div 4 \approx 1 \text{ (s)}$

Table 13. Scroll mode and scroll resolution

Mode	Scroll resolution	Scroll speed
Mode 1	1 H Unit	about 4 second
	2 H Unit	about 2 second
Mode 2	4 H Unit	about 1 second
Mode 3	4 H Unit	about 1 second

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**INTERRUPT INTERVAL DETERMINATION
FUNCTION**

The M37102M8-XXXSP incorporates an interrupt interval determination circuit. This interrupt interval determination circuit has an 8-bit binary counter as shown in Figure 40. Using this counter, it determines a duration of time from the rising transition (falling transition) of an input signal pulse on the INT₁ or INT₂ to the rising transition (falling transition) of the signal pulse that is input next.

The following describes how the interrupt interval is determined.

1. The interrupt input to be determined (INT₁ input or INT₂ input) is selected by using bit 2 in the interrupt interval determination control register (address 00D8₁₆). When this bit is cleared to "0", the INT₁ input is selected; when the bit is set to "1", the INT₂ input is selected.
2. When the INT₁ input is to be determined, the polarity is selected by using bit 3 in the interrupt interval determination control register; when the INT₂ input is to be determined, the polarity is selected by using bit 4 in the interrupt interval determination control register. When the relevant bit is cleared to "0", determination is made of the interval of a positive polarity (rising transition); when the bit is set to "1", determination is made of the interval of a negative polarity (falling transition).
3. The reference clock is selected by using bit 1 in the interrupt interval determination control register. When the bit is cleared to "0", a 64 μ s clock is selected; when the bit is set to "1", a 32 μ s clock is selected (based on an oscillation frequency of 4MHz in either case).
4. Simultaneously when the input pulse of the specified polarity (rising or falling transition) occurs on the INT₁ pin (or INT₂ pin), the 8-bit binary counter starts counting up with the selected reference clock (64 μ s or 32 μ s).
5. Simultaneously with the next input pulse, the value of the 8-bit binary counter is loaded into the determination register (address 00D7₁₆) and the counter is immediately reset (00₁₆). The reference clock is input in succession even after the counter is reset, and the counter restarts counting up from "00₁₆".
6. When count value "FE₁₆" is reached, the 8-bit binary counter stops counting. Then, simultaneously when the reference clock is input next, the counter sets value "FF₁₆" to the determination register.

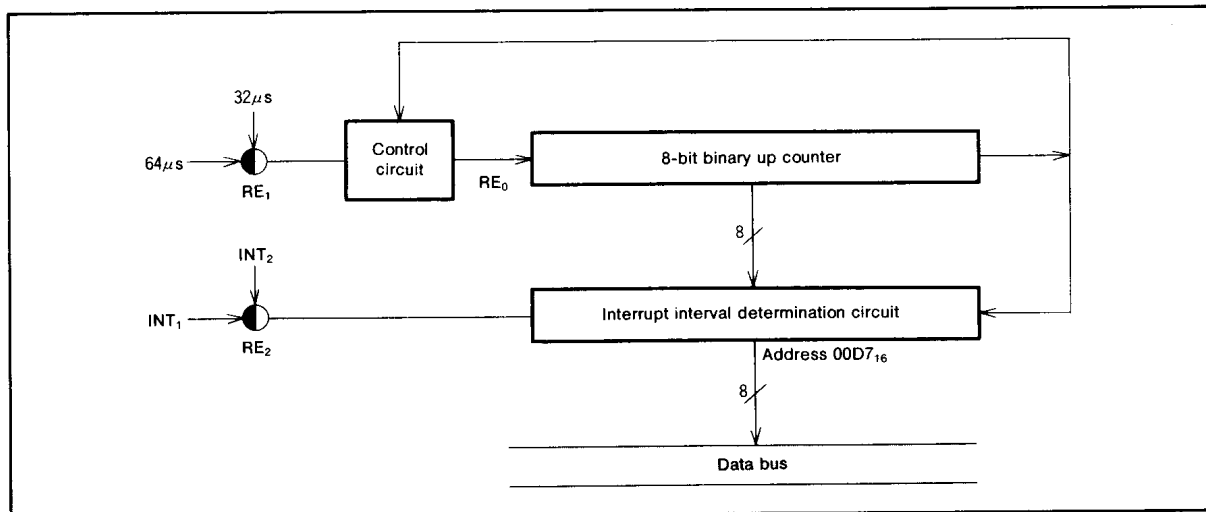


Fig. 40 Block diagram of interrupt interval determination circuit

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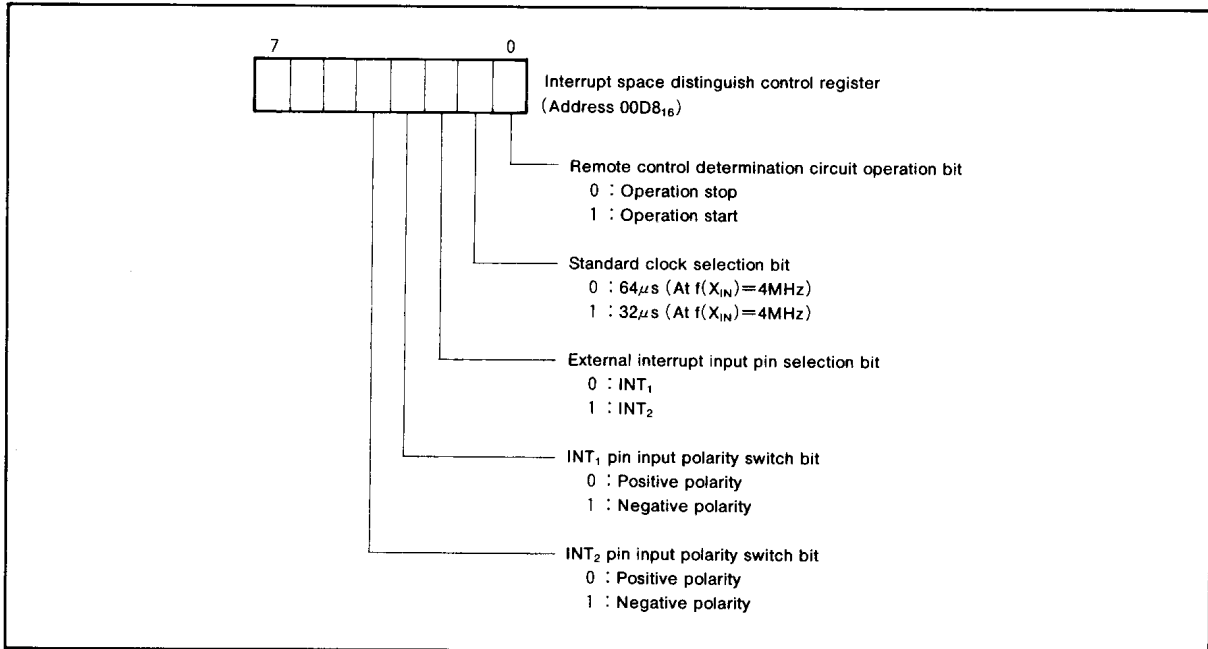


Fig. 41 Structure of interrupt space distinguish control register

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RESET CIRCUIT

The M37102M8-XXXSP is reset according to the sequence shown in Figure 44. It starts the program from the address formed by using the content of address $FFFF_{16}$ as the high order address and the content of the address $FFFE_{16}$ as the low order address, when the RESET pin is held at "L" level for no less than $2\mu s$ while the power voltage is $5V \pm 10\%$

and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 42.

An example of the reset circuit is shown in Figure 43. The reset input voltage must be kept below 0.6V until the supply voltage surpasses 4.5V.

	Address	Contents
(1) Port P0 directional register	(00C1 ₁₆)...	00 ₁₆
(2) Port P1 directional register	(00C3 ₁₆)...	00 ₁₆
(3) Port P2 directional register	(00C5 ₁₆)...	00 ₁₆
(4) Port P3 directional register	(00C7 ₁₆)...	00 ₁₆
(5) Port P4 directional register	(00C9 ₁₆)...	00 ₁₆
(6) Port P5 directional register	(00CB ₁₆)...	000000
(7) Port P6 directional register	(00CD ₁₆)...	00 ₁₆
(8) PWM output control register 1	(00D5 ₁₆)...	00 ₁₆
(9) PWM output control register 2	(00D6 ₁₆)...	00 ₁₆
(10) Interrupt space distinguish control register	(00D8 ₁₆)...	00 ₁₆
(11) Special mode register 1	(00DA ₁₆)...	00 ₁₆
(12) Special mode register 2	(00DB ₁₆)...	00 ₁₆
(13) Serial I/O1 mode register	(00DC ₁₆)...	00 ₁₆
(14) Serial I/O2 mode register	(00DE ₁₆)...	00 ₁₆
(15) Horizontal position register	(00E0 ₁₆)...	00000000
(16) Color register 0	(00E6 ₁₆)...	00 ₁₆
(17) Color register 1	(00E7 ₁₆)...	00 ₁₆
(18) Color register 2	(00E8 ₁₆)...	00 ₁₆
(19) Color register 3	(00E9 ₁₆)...	00 ₁₆
(20) CRT control register	(00EA ₁₆)...	00 ₁₆
(21) Display block counter	(00EB ₁₆)...	0000
(22) Polarity register	(00EC ₁₆)...	00 ₁₆
(23) Scroll control register	(00ED ₁₆)...	00000000
(24) A-D control register	(00EF ₁₆)...	00000000
(25) Timer 1	(00F0 ₁₆)...	FF ₁₆
(26) Timer 2	(00F1 ₁₆)...	07 ₁₆
(27) Timer 3	(00F2 ₁₆)...	FF ₁₆
(28) Timer 4	(00F3 ₁₆)...	07 ₁₆
(29) Timer 12 mode register	(00F4 ₁₆)...	000000
(30) Timer 34 mode register	(00F5 ₁₆)...	0000
(31) CPU mode register	(00FB ₁₆)...	11111100
(32) Interrupt request register 1	(00FC ₁₆)...	000000
(33) Interrupt request register 2	(00FD ₁₆)...	000000
(34) Interrupt control register 1	(00FE ₁₆)...	000000
(35) Interrupt control register 2	(00FF ₁₆)...	000000
(36) Processor status register	(PS)	1
(37) Program counter	(PC _H)	Contents of address FFFF ₁₆
	(PC _L)	Contents of address FFFE ₁₆

Note : Since the contents of both registers other than those listed above and the RAM are undefined at reset, it is necessary to set initial values.
At reset, "0" is read from all bits which is not used.

Fig. 42 Internal state of microcomputer at reset

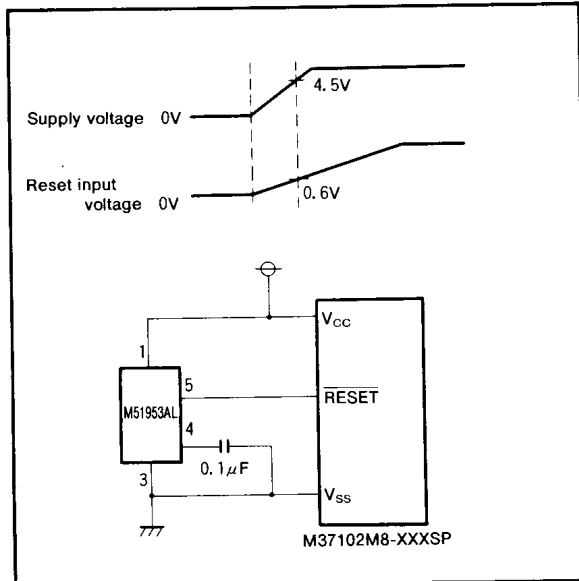


Fig. 43 Example of reset circuit

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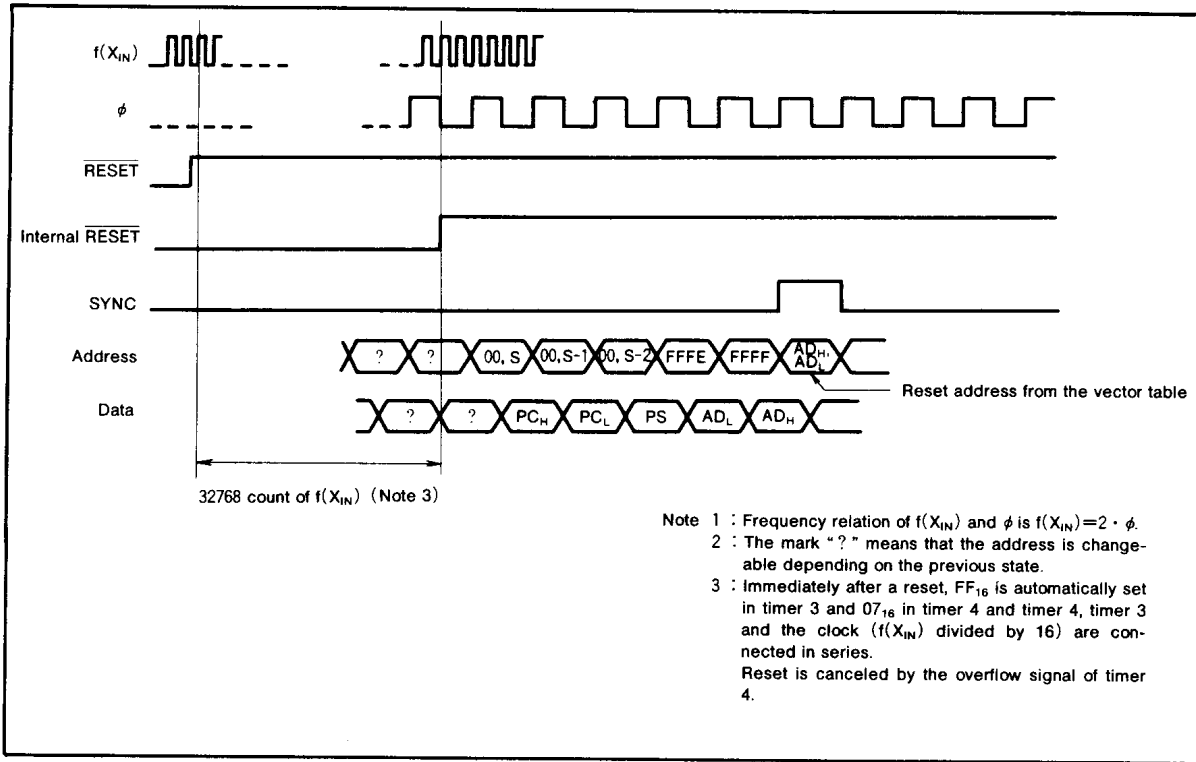


Fig. 44 Timing diagram at reset

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I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with CMOS output.

As shown in the memory map (Figure 2), port P0 can be accessed at zero page memory address $00C0_{16}$.

Port P0 has a directional register (address $00C1_{16}$) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously output value to be read correctly even though the output voltage level is shifted up or down. Pins set as input are in the floating state and the signal levels can thus be read. When data is written into the input port, the data is latched only to the port latch and the pin still remains in the floating state.

Depending on the contents of the processor mode bits (bit 0 and bit 1 at address $00FB_{16}$), three different modes can be selected; single-chip mode, memory expanding mode and microprocessor mode.

In these modes it functions as address ($A_7 \sim A_0$) output port (excluding single-chip mode). For more details, see the processor mode information.

(2) Port P1

In single-chip mode, port P1 has the same function as port P0. In other modes, it functions as address ($A_{15} \sim A_8$) output port.

Refer to the section on processor modes for details.

(3) Port P2

In single-chip mode, port P2 has the same function as port P0. In other modes, it functions as data ($D_0 \sim D_7$) input/output port. Refer to the section on processor modes for details.

(4) Port P3

Port P3 is an 7-bit I/O port with function similar to port P0, but the output structure of $P3_0, P3_1$ is CMOS output and $P3_2 \sim P3_6$ is N-channel open drain.

$P3_2, P3_3$ are in common with the external clock input pins of timer 2 and 3.

$P3_4, P3_6$ are in common with the external interrupt input pins INT_1, INT_2 and $P3_5, P3_6$ with the analog input pins of A-D converter A-D₁, A-D₂.

In the microprocessor mode or the memory expanding mode, $P3_0, P3_1$ works as R/W signal output pin and SYNC signal output pin.

(5) Port P4

Port P4 is an 8-bit I/O port with function similar to port P0, but the output structure is N-channel open drain output.

All pins have program selectable dual functions. When a serial I/O 1 function is selected, $P4_0 \sim P4_3$ work as input/output pins of serial I/O1. When a serial I/O2 function is selected, $P4_4 \sim P4_7$ work as input/output pins of serial I/O2.

In the special serial I/O mode, $P4_4, P4_5$ work as SDA, SCL pins. $P4_6, P4_7$ are in common with PWM8 and 9 output pins.

(6) OSC1, OSC2 pins

Clock input/output pins for CRT display function.

(7) H_{SYNC}, V_{SYNC} pins

H_{SYNC} is a horizontal synchronizing signal input pin for CRT display.

V_{SYNC} is a vertical synchronizing signal input pin for CRT display.

(8) R, G, B, I, OUT pins

This is an 5-bit output pin for CRT display and in common with $P5_2 \sim P5_6$.

(9) Port P6

Port P6 is an 8-bit I/O port with function similar to port P0, but the output structure is N-channel open drain output.

This port is in common with 8-bit PWM output pin PWM0~PWM7.

(10) D-A pin

This is a 14-bit PWM output pin.

(11) ϕ pin

The internal system clock (1/4 the frequency of the oscillator connected between the X_{IN} and X_{OUT} pins) is output from this pin. If an STP or WIT instruction is executed, output stops after going "H".

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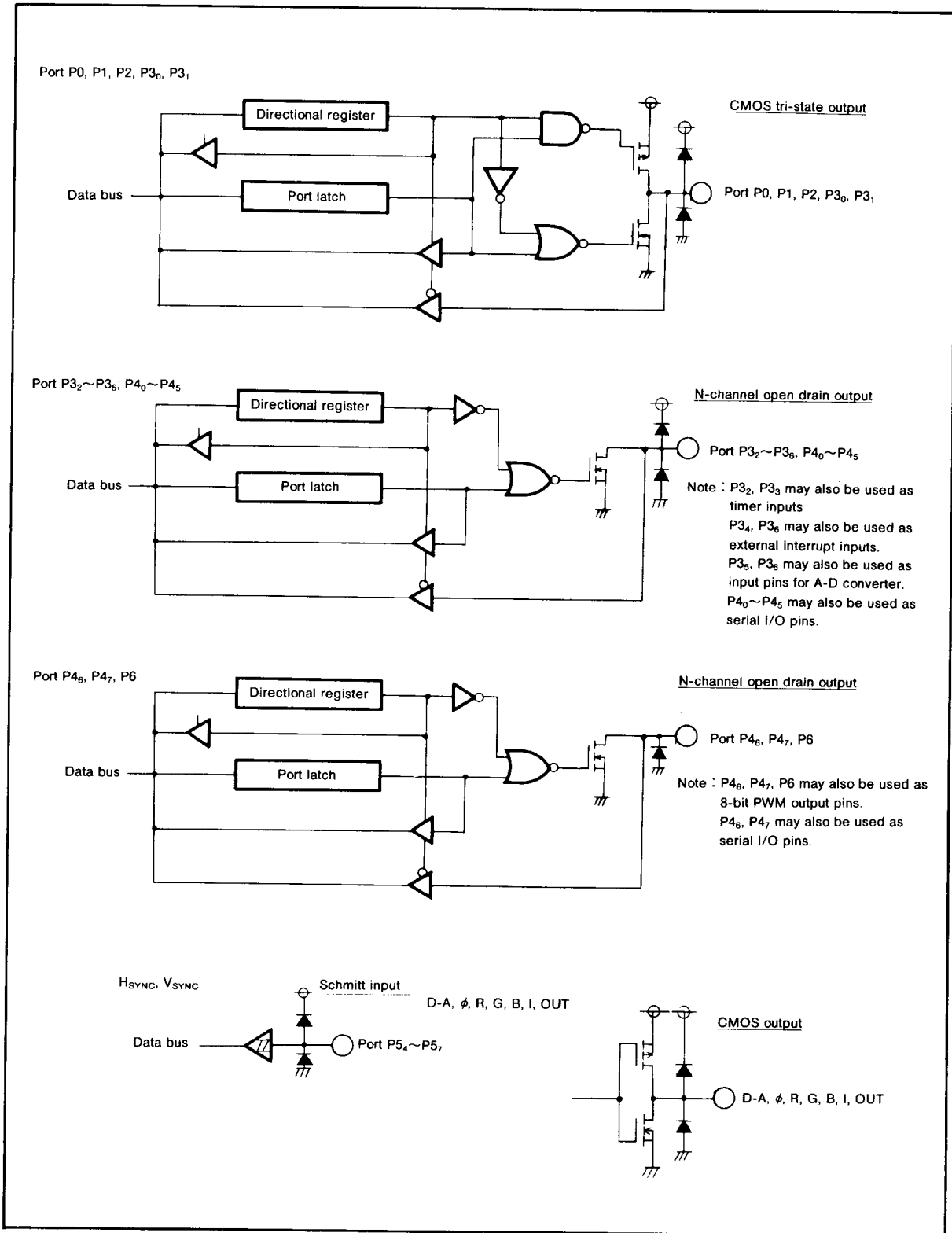


Fig. 45 Block diagram of port P0~P6 (single-chip mode) and output format of D-A, φ, R, G, B, I, OUT

MITSUBISHI MICROCOMPUTERS
M37102M8-XXXSP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER for VOLTAGE SYNTHESIZER
with ON-SCREEN DISPLAY CONTROLLER

PROCESSOR MODE

By changing the contents of the processor mode bit (bit 0 and 1 at address 00FB₁₆), three different operation modes can be selected; single-chip mode, memory expanding mode, and microprocessor mode.

In the memory expanding mode and the microprocessor mode, ports P0~P3 can be used as address, and data input/output pins.

Figure 47 shows the functions of ports P0~P3.

The memory map for the single-chip mode is illustrated in Figure 1 and for other modes, in Figure 46.

By connecting CNV_{SS} to V_{SS}, all three modes can be selected through software by changing the processor mode bits. Connecting CNV_{SS} to V_{CC} automatically forces the microcomputer into memory expanding mode.

The three different modes are explained as follows:

(1) Single-chip mode {00}

The microcomputer will automatically be in the single-chip mode when started from reset, if CNV_{SS} is connected to V_{SS}. Ports P0~P3 will work as original I/O ports.

(2) Memory expanding mode {01}

The microcomputer will be placed in the memory expanding mode after connecting CNV_{SS} to V_{CC} and initiating a reset or connecting CNV_{SS} to V_{SS} and the processor mode bits are set to "01". This mode is used to add external memory when the internal memory is not sufficient.

In this mode, port P0 and port P1 are as a system address bus and the original I/O pin function is lost.

Port P2 becomes the data bus of D₇~D₀ (including instruction code) and loses its normal I/O function. Port P_{3,0} and P_{3,1} works as R/W and φ.

(3) Microprocessor mode {10}

When CNV_{SS} is connected to V_{SS} and the processor mode bits are set to "10", the microcomputer will automatically default to this mode. In this mode, the internal ROM is inhibited so the external memory is required. Other functions are same as the memory expanding mode. The relationship between the input level of CNV_{SS} and the processor mode is shown in Table 14.

Note : Use the M37102M8-XXXSP in the microprocessor mode or the memory expanding mode only at program development.

The standards is assured only in the single-chip mode.

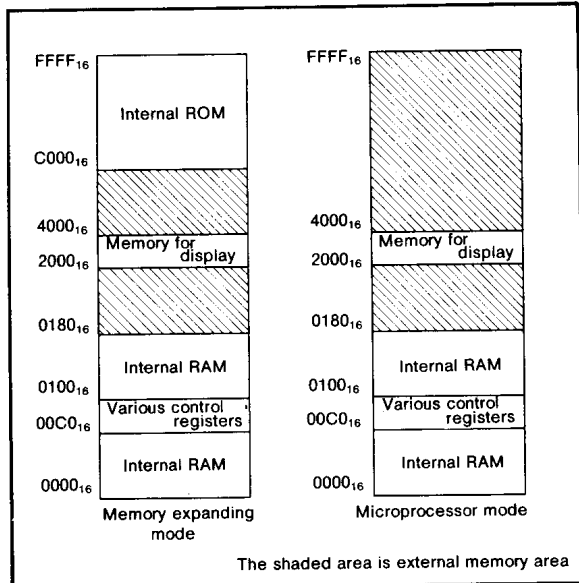


Fig. 46 Example memory area in processor mode

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	CM ₁	0	0	1
	CM ₀	0	1	0
Mode		Single-chip mode	Memory expanding mode	Microprocessor mode
Port				
Port P0				Same as left
Port P1				Same as left
Port P2				Same as left
Port P3				Same as left

Fig. 47 Processor mode and function of port P0~P3

Table 14. Relationship between CNV_{SS} pin input level and processor mode

CNV _{SS}	Mode	Explanation
V _{SS}	<ul style="list-style-type: none"> • Single-chip mode • Memory expanding mode • Microprocessor mode 	The single-chip mode is set by the reset. All modes can be selected by changing the processor mode bit with the program.
V _{CC}	<ul style="list-style-type: none"> • Memory expanding mode 	The memory expanding mode is set by the reset

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CLOCK GENERATING CIRCUIT

The built-in clock generating circuits are shown in Figure 50.

When an STP instruction is executed, the internal clock ϕ stops oscillating at "H" level. At the same time, timer 3 and timer 4 are connected automatically and FF_{16} is set in the timer 3, 03_{16} is set in the timer 4, and timer 3 count source is forced to $f(X_{IN})$ divided by 16. This connection is cleared when an external interrupt is accepted or the reset is in, as discussed in the timer section.

The oscillator is restarted when an interrupt is accepted. However, the clock ϕ keeps its "H" level until timer 4 overflows.

This is because the oscillator needs a set-up period if a ceramic or a quartz crystal oscillator is used.

When the WIT instruction is executed, the clock ϕ stops in the "H" level but the oscillator continues running. This wait state is cleared when an interrupt is accepted. Since the oscillation does not stop, the next instructions are executed at once.

To return from the stop or the wait status, the interrupt enable bit must be set to "1" before executing STP or WIT instruction.

The circuit example using a ceramic oscillator (or a quartz crystal oscillator) is shown in Figure 48.

The constant capacitance will differ depending on which oscillator is used, and should be set to the manufactures suggested value.

The example of external clock usage is shown in Figure 49. X_{IN} is the input, and X_{OUT} is open.

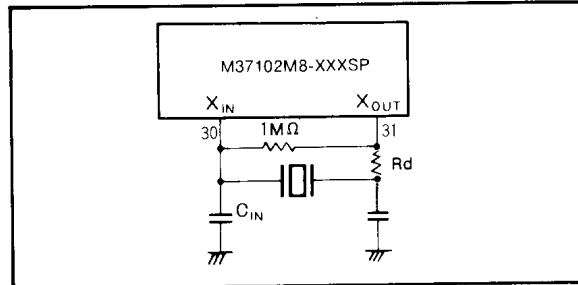


Fig. 48 External ceramic resonator circuit

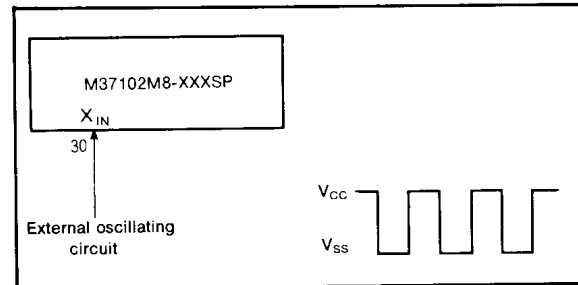


Fig. 49 External clock input circuit

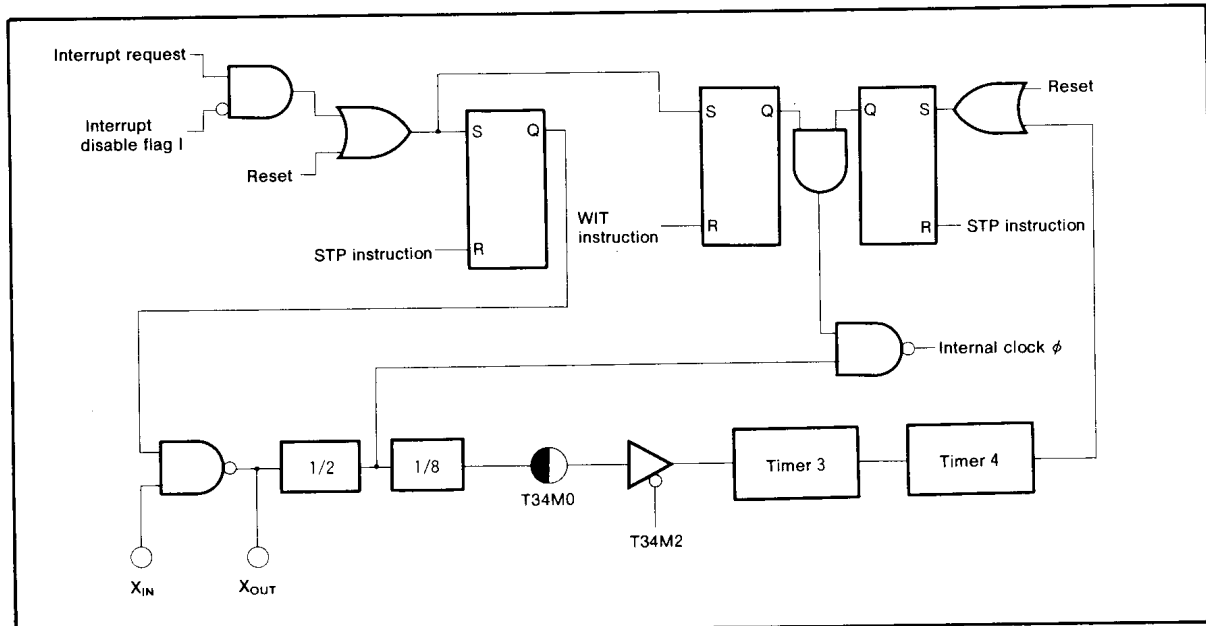


Fig. 50 Block diagram of clock generating circuit

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PROGRAMMING NOTES

- (1) The frequency ratio of the timer is $1/(n+1)$.
- (2) Even though the BBC and BBS instructions are executed after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modifications are only valid for the contents before the modification. Also, at least one instruction cycle must be used (such as a NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
- (3) After the ADC and SBC instructions are executed (in decimal mode), one instruction cycle (such as a NOP) is needed before the SEC, CLC, or CLD instructions are executed.
- (4) A NOP instruction must be used after the execution of a PLP instruction.
- (5) In order to avoid noise and latch-up, connect a bypass capacitor ($\approx 0.1\mu F$) directly between the V_{CC} pin and V_{SS} pin using a heavy wire.

DATA REQUIRED FOR MASK ORDERING

Please send the following data for mask orders.

- (1) mask ROM order confirmation form
- (2) mask specification form
- (3) ROM data EPROM 3 sets

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{CC}	Supply voltage		-0.3~6	V
V _I	Input voltage CNV _{SS}		-0.3~6	V
V _I	Input voltage P ₀ ~P ₀₇ , P ₁ ~P ₁₇ , P ₂ ~P ₂₇ , P ₃ ~P ₃₆ , P ₄ ~P ₄₇ , P ₆ ~P ₆₇ , H _{SYNC} , V _{SYNC} , RESET	With respect to V _{SS} Output transistors are at "off" state.	-0.3~V _{CC} +0.3	V
V _O	Output voltage P ₀ ~P ₀₇ , P ₁ ~P ₁₇ , P ₂ ~P ₂₇ , P ₃ ~P ₃₆ , P ₄ ~P ₄₇ , P ₆ ~P ₆₇ , R, G, B, I, OUT, D-A, X _{OUT} , OSC2		-0.3~V _{CC} +0.3	V
I _{OH}	Circuit voltage R, G, B, I, OUT, P ₀ ~P ₀₇ , P ₁ ~P ₁₇ , P ₂ ~P ₂₇ , P ₃ ~P ₃₆ , P ₄ ~P ₄₇ , D-A		0~1 (Note 1)	mA
I _{OL1}	Circuit voltage R, G, B, I, OUT, P ₀ ~P ₀₇ , P ₁ ~P ₁₇ , P ₂ ~P ₂₇ , P ₃ ~P ₃₆ , P ₄ ~P ₄₇ , D-A		0~1 (Note 2)	mA
I _{OL2}	Circuit voltage P ₆ ~P ₆₇ , P ₄ ~P ₄₇		0~1 (Note 2)	mA
I _{OL3}	Circuit voltage P ₂ ~P ₂₇		0~10 (Note 3)	mA
P _d	Power dissipation	T _a =25°C	550	mW
T _{opr}	Operating temperature		-10~70	°C
T _{stg}	Storage temperature		-40~125	°C

RECOMMENDED OPERATING CONDITIONS (V_{CC}=5V±10%, T_a=-10~70°C unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V _{CC}	Supply voltage (Note 4) During the CRT operation	4.5	5.0	5.5	V
V _{SS}	Supply voltage	0	0	0	V
V _{IH}	"H" input voltage P ₀ ~P ₀₇ , P ₁ ~P ₁₇ , P ₂ ~P ₂₇ , P ₃ ~P ₃₆ , P ₄ ~P ₄₇ , P ₆ ~P ₆₇ , H _{SYNC} , V _{SYNC} , RESET, X _{IN} , OSC1	0.8V _{CC}		V _{CC}	V
V _{IH}	"H" input voltage P ₄ , P ₅	0.7V _{CC}		V _{CC}	V
V _{IL}	"L" input voltage P ₀ ~P ₀₇ , P ₁ ~P ₁₇ , P ₂ ~P ₂₇ , P ₃ ~P ₃₆ , P ₄ ~P ₄₇ , P ₆ ~P ₆₇	0		0.4V _{CC}	V
V _{IL}	"L" input voltage P ₃ ~P ₃₆ , P ₄ ~P ₄₇ , P ₆ ~P ₆₇ , H _{SYNC} , V _{SYNC} , RESET, X _{IN} , OSC1	0		0.2V _{CC}	V
I _{OH}	"H" average output current (Note 1) R, G, B, I, OUT, P ₀ ~P ₀₇ , P ₁ ~P ₁₇ , P ₂ ~P ₂₇ , P ₃ ~P ₃₆ , P ₄ ~P ₄₇			1	mA
I _{OL1}	"L" average output current (Note 2) R, G, B, I, OUT, P ₀ ~P ₀₇ , P ₂ ~P ₂₇ , P ₃ ~P ₃₆ , P ₄ ~P ₄₇ , D-A			2	mA
I _{OL2}	"L" average output current (Note 2) P ₆ ~P ₆₇ , P ₄ ~P ₄₇			1	mA
I _{OL3}	"L" average output current (Note 3) P ₂ ~P ₂₇			10	mA
f _{CPU}	Oscillating frequency (for CRT operation) (Note 5)	3.6	4.0	4.4	MHz
f _{CRT}	Oscillating frequency (for CRT display)	6.0	7.0	8.0	MHz
f _{hs}	Input frequency P ₃ ~P ₃₆ , P ₄ ~P ₄₇			100	kHz
f _{hs}	Input frequency P ₄			1	MHz

- Note 1 : The total current that flows out of the IC should be 20mA (max.).
 2 : The total of I_{OL1} and I_{OL2} should be 30mA (max.).
 3 : The total of I_{OL} of port P₂~P₂₇ should be 20mA (max.).
 4 : Apply 0.022μF or greater capacitance externally between the V_{CC}-V_{SS} power supply pins so as to reduce power source noise.
 Also apply 0.068μF or greater capacitance externally between the V_{CC}-CNV_{SS} pins.

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ELECTRIC CHARACTERISTICS ($V_{CC}=5V\pm 10\%$, $V_{SS}=0V$, $T_a=-10\sim 70^\circ C$, $f(X_{IN})=4MHz$ unless other wise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CC}	Supply current	$V_{CC}=5.5V$, $f(X_{IN})=4MHz$ CRT OFF		10	20	mA
		$V_{CC}=5.5V$, $f(X_{IN})=4MHz$ CRT ON		20	30	
		At stop mode			300	μA
V_{OH}	"H" output voltage $P0_0\sim P0_7$, $P1_0\sim P1_7$, $P2_0\sim P2_7$, $P3_0$, $P3_1$, R, G, B, I, OUT	$V_{CC}=4.5V$ $I_{OH}=-0.5mA$	2.4			V
V_{OL}	"L" output voltage $P0_0\sim P0_7$, $P1_0\sim P1_7$, $P2_0\sim P2_3$, $P3_0\sim P3_6$, $P4_0\sim P4_3$, R, G, B, I, OUT, D-A	$V_{CC}=4.5V$ $I_{OL}=0.5mA$			0.4	V
	"L" output voltage $P6_0\sim P6_7$, $P4_6$, $P4_7$	$V_{CC}=4.5V$ $I_{OL}=0.1mA$			0.4	
	"L" output voltage $P2_4\sim P2_7$	$V_{CC}=4.5V$ $I_{OL}=10mA$			3.0	
	"L" output voltage $P4_4$, $P4_5$	$V_{CC}=4.5V$ $I_{OL}=3mA$			0.4	
$V_{T+}-V_{T-}$	Hysteresis RESET	$V_{CC}=5.0V$		0.5	0.7	V
	Hysteresis (Note 6) H_{SYNC} , V_{SYNC} , $P3_2\sim P3_4$, $P3_6$, $P4_1$, $P4_2$, $P4_4\sim P4_6$	$V_{CC}=5.0V$		0.5	1.3	
I_{OZH}	"H" input leak current RESET, $P0_0\sim P0_7$, $P1_0\sim P1_7$, $P2_0\sim P2_7$, $P3_0\sim P3_6$, $P4_0\sim P4_5$	$V_{CC}=5.5V$ $V_O=5.5V$			5	μA
	"H" input leak current $P6_0\sim P6_7$, $P4_6$, $P4_7$	$V_{CC}=5.5V$ $V_O=5.5V$			10	
I_{OZL}	"L" input leak current RESET, $P0_0\sim P0_7$, $P1_0\sim P1_7$, $P2_0\sim P2_7$, $P3_0\sim P3_6$, $P4_0\sim P4_7$, $P6_0\sim P6_7$	$V_{CC}=5.5V$ $V_O=0V$			5	μA

Note 1. $P3_2\sim P3_4$, $P3_6$ have the hysteresis when these pins are used as interrupt input pins or timer input pins.
 $P4_1$, $P4_2$, $P4_4\sim P4_6$ have the hysteresis when these pins are used as serial I/O ports.

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